# Senior Design

## Frequency Resolved Electrical Gating Device to Measure Ultrashort Optical Pulses

## College of Electrical Engineering and Computer Science

## College of Optics and Photonics

University of Central Florida
Dr. ChungYong Chan
Dr. Aravinda Kar

# Group 2 CREOL

Namisha Jagmohan - Photonic Science & Engineering, Electrical Engineering

Odane Lennox - Electrical Engineering

Keana Paredes - Photonic Science and Engineering

Alex Wheat – Computer Engineering

Project Advisor: Andrea Blanco-Redondo

Project Committee: Andrea Blanco-Redondo, Nazanin Rahnavard, Avra Kundu

# Contents

# Table of Figures

# Index of Tables

# Chapter 1 Executive Summary

The proposed project is an apparatus for the characterization of ultra-short, low energy optical pulse trains to measure their pulse amplitude and phase. This apparatus is necessary as ultra-short optical pulses, specifically those on the order of a few picoseconds in duration, cannot be measured by typical photodetectors alone. This is due to limits in photodetector electrical response times with respect to electron transit time and inherent capacitances and resistances within the device circuitry. Additionally, the optical pulses we are interested in characterizing are low energy (<40 pJ); Because of this, we cannot use well-established means, such as Frequency-Resolved Optical Gating (FROG), to retrieve the pulse amplitude and phase. Thus, to circumvent the limits of electronic circuitry and detect these low-energy pulses, we aim to build a FREG (Frequency-Resolved Electrical Gating) system.

The FREG requires supporting hardware and software to function independently, namely an optical spectrum analyzer, a blind deconvolution algorithm, and a custom PCB. The spectrum analyzer allows us to build a spectrogram from the output optical signals of the FREG. The blind deconvolution algorithm then takes that spectrogram and deconvolves it so we can retrieve the pulse information. The microcontroller on the PCB handles communications between the FREG, spectrum analyzer, and the computer. The design of these sub-systems will also be detailed in this paper.

The software used in the system has 2 distinct portions: embedded software which controls the microcontroller and a computer program which the user interacts with. The embedded software handles the FREG hardware by communicating the necessary data between components as well as directly controlling other components. The computer program lets the user begin the pulse retrieval process and view the results. This involves first acquiring data from the FREG hardware and assembling it into a usable format. The deconvolution is then performed using complex math, and the characterization data is displayed to the user as the results of the process.

A Multi-layer PCB integration will be incorporated into the FREG system to ensure proper power distribution and establishment of various communications links. The time delay line and the PC consist of a USB 2.0 port connection to the Microcontroller. Implementing a USB-to-UART bridge converter is important for relaying and receiving data for both interfaces. The precision motor is the third major aspect of the system that requires incorporating a designed PWM controller to send instructions from the MCU based on the data received by the time delay line. Design techniques for lowering the impedance of the board will be included as the PCB contains high-speed components which can lead to malfunctions and faults in the routing of the traces if ignored. Calculations and comparisons on different components will be carefully analyzed to determine the optimal circuit designs necessary to meet all parameters of the FREG system without compromising on performance.

# Chapter 2 Project Description

## 2.1 Motivation

The motivation for ultra-short, low-energy optical pulses in these devices is due to their use in the telecommunications and medical domains. Ultra-short optical pulses are necessary for pushing bit rates higher, as the shorter the pulses are, the more bits can be transmitted per second.

This is important as data throughout needs increase exponentially with each year. Additionally, these optical pulses for communications are low energy, on the order of picojoules to femtojoules, and are thus low-power pulses (~10 μW) when factoring in their short durations. This is important for power consumption. The motivation for characterizing such ultra-short, low-energy pulsed sources regarding the medical domain is for use in optical biopsies and ophthalmology. Essentially, these sources can cut tissue without damaging it during surgeries.

Thus overall, the FREG apparatus accomplishes two goals for the customer: It returns the amplitude of a pulse, as well as its phase. These attributes of the pulse are necessary to retrieve, as knowing these properties helps us counteract dispersion of the pulses as they propagate through the systems they will be implemented into. Measuring amplitude is important for achieving the desired high data transmission rates. This is because pulse amplitude also tells us about its duration. The relevance of the phase of these optical pulses is that it is needed for mitigating signal degradation due to intramodal dispersion. [1]

## 2.2 Background

The FREG is a successor to the more commonly known FROG (Frequency-Resolved Optical Gating) system. However, the FROG setup is unideal for our application due to its need for nonlinear optical pulse mixing, which requires high-energy pulses. The FREG's desired application will mainly be for the characterization of optical pulse outputs from fiber lasers and photonic crystal waveguides which will be outputting low-energy optical pulses. The FREG's ability to resolve ultra-short pulses without the need for non-linear optical pulse mixing makes the system much more sensitive compared to FROG, to the extent that it is able to accurately measure pulses which contain less than 100 photons. [2]

The primary concept of the FREG is taking advantage of convolution theory to make a difficult measurement in the time-domain obtainable. This is done via pulse interference, signal conversion to the frequency domain, and a subsequent deconvolution algorithm to extract pulse duration and phase. The system utilizes signal gating to create a 2D spectrogram of the device-under-test's (DUT's) impulse response behavior. The input signal with a varying time delay is what we call the "gating" function, as the amount of delay determines the pulse-overlap and subsequent intensity modulation in the FREG output.

We will now discuss the overall system set-up. We begin with the input. As seen in Figure 1, the input we will be testing the FREG system with is a mode-locked laser. There may be other inputs, depending on what the user would like to characterize. A mode-locked laser outputs short optical pulses in the time domain, which are often referred to as a pulse train. This output light is not continuously flowing (or continuous wave), but instead switches on and off. These optical pulses have a consistent amplitude and phase which we are interested in retrieving. The pulse amplitude will tell us the width of the pulse as well. The repetition rate of a laser is how many pulses are emitted per second. The inverse of the repetition rate tells us the period of the laser output, or the pulse-to-pulse duration. This information is described in Figure 1.

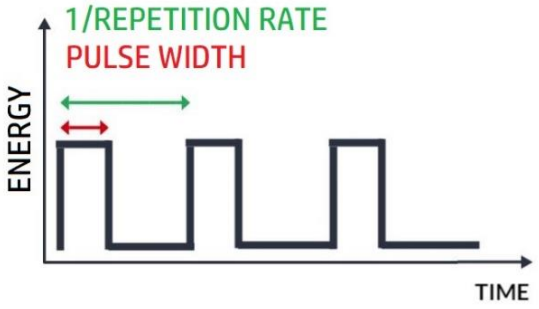



Figure 1: Optical Pulse Train. Shows a pulse train and relevant attributes such as the repetition rate, pulse width, and pulse energy. The periodic nature of the input pulse train is vital to the FREG's ability to retrieve the pulse amplitude and phase.

For the sake of simplicity, we are going to look at a singular pulse in this pulse train for our analysis through the FREG. This assumption does not impact any analyses of the FREG functionality, because of the periodic nature of the signals being used. We can also make this assumption because the pulse width will generally be much smaller than the inverse of the repetition rate (i.e. the pulse-to-pulse duration). For the following explanation of the device's operation, we will be referring to Figure 2 in conjunction with Figures 4a and 4b. There is numbering on the figures to keep track of important locations.

The optical signal/pulse first propagates into the system. When it reaches the beamsplitter, the optical energy is split into a given ratio, dependent on the beam splitter which is chosen. For the purposes of this explanation, we will assume that it transmits 90% of the light into the reference arm and 10% of the light into the secondary arm. After this beamsplitter is position 1 defined on Figures 2 and 6. We see that there are two pulses, with different fractions of the incident power.

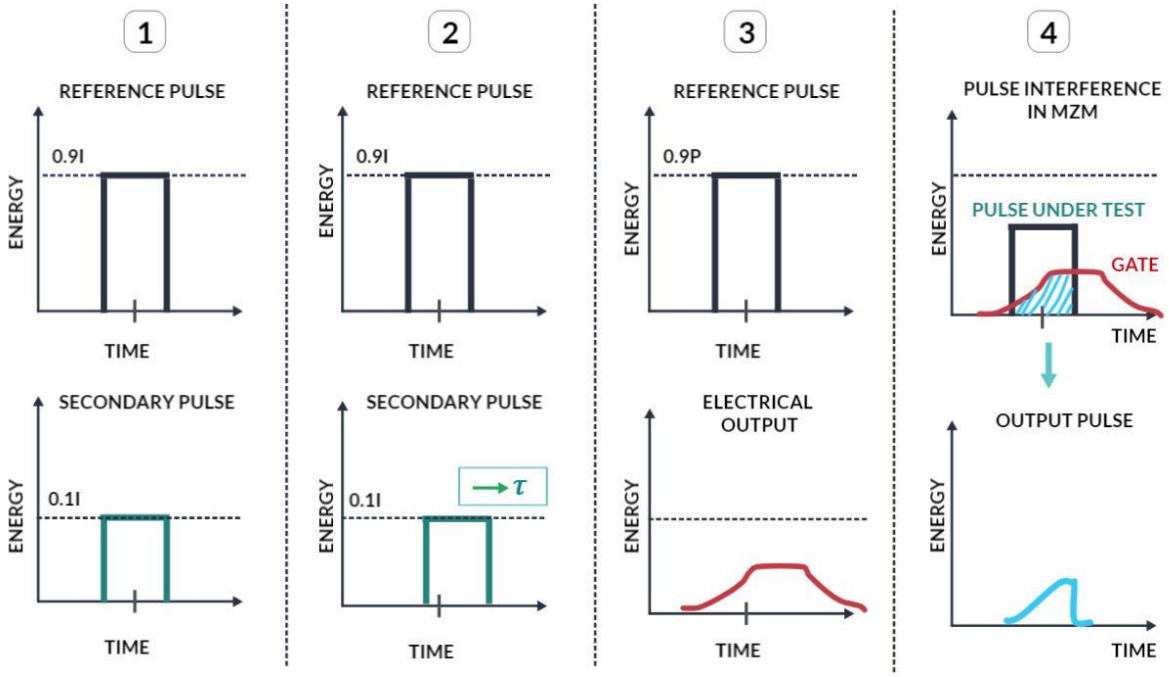


Figure 2: FREG Snapshots. Shows “snapshots” of the signals through the reference arm and secondary arm at different locations in the system. We can see the transformation of the secondary pulse and its subsequent recombination with the reference pulse.

The pulses continue propagating. For clarity, the entire system is connectorized via optical fiber, it is not free-space propagating, as this would introduce more losses and noise. The reference pulse continues propagating through fiber and experiences no changes. The secondary pulse however, encounters the variable time delay line. This component introduces a change in the optical path length within the secondary arm. This delay line is adjustable. Thus, the secondary pulse is shown to be delayed in time with respect to the original pulse at point 2, because the secondary pulse had to travel an extended distance.

We then reach point 3, where the propagation of the secondary signal gets more complicated. The reference signal remains the same, still propagating through the fiber. The secondary signal encounters a fast photodiode, where the optical signal is converted to an electrical signal. These optical pulses are on the femtosecond scale, which far exceeds the electrical bandwidth of the photodiode. This means that the photodiode cannot respond to the optical signal accurately, and thus does not produce an electrical signal that is 1:1, or a copy, of the optical signal. Instead, the input signal becomes elongated, as seen in Figure 2 at position 3 for the secondary arm.

This electrical signal from the photodiode is then used as an input to the electro-optic Mach-Zehnder modulator. The set-up of a Mach-Zehnder Modulator is shown below. It has an optical input, optical output, a DC bias, and an RF input. The optical pulse from the reference arm is the optical input. The modulator structure splits incoming optical energy 50/50 into two waveguides, one of which has a voltage applied to it which is the RF input from the photodiode.

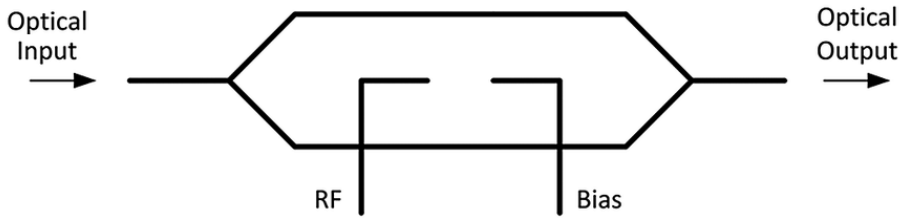



Figure 3: MZM Structure. Shows a basic top-view representation of an MZM. The optical input is split into two arms, one of which is under a DC bias and is driven by an input RF signal. When the signals are recombined at the Y-junction, any differences in phase as well as how much the pulses are overlapped will determine the amplitude modulation.

When the RF input is applied to an arm of the modulator, this electric field changes the refractive index minutely. This change in refractive index means the light will travel either slower or faster through one of the arms of the device. These optical signals are recombined at the end of the device, where their differences in phase modulates the amplitude of the final optical signal. This is what we see at point 4. This recombination is where the pulse overlapping occurs, giving us the final output of the FREG. This overall process within the FREG is repeated for many different time delays, as seen in Figure 4b, so that we can build a spectrogram similar to the one seen in Figure 5a.

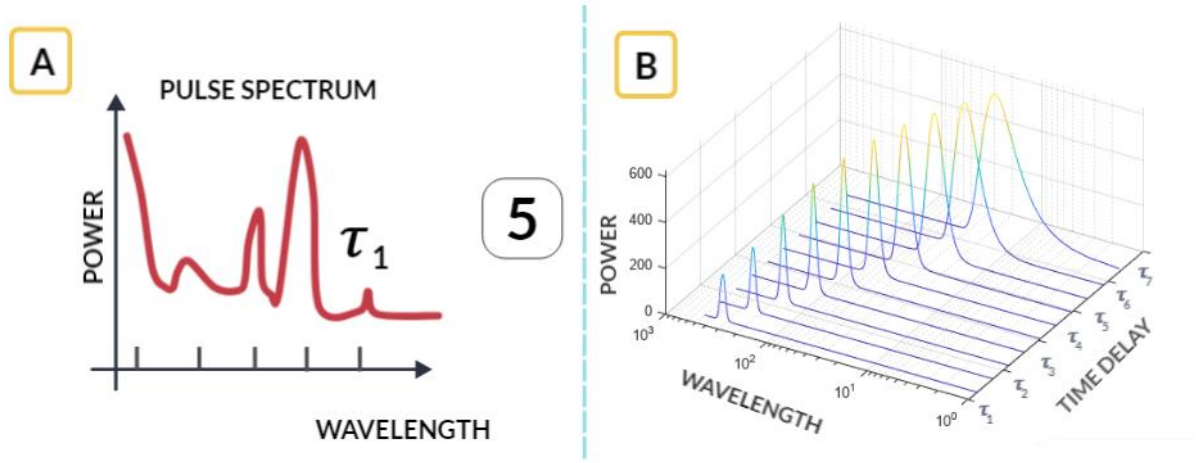
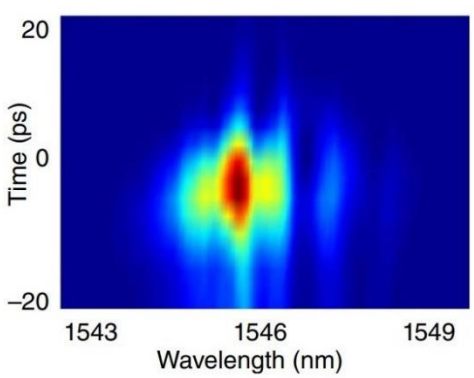



Figure 4a (Left): 2D Spectrum Example. Shows an example of what a pulse spectrum would look like. This is necessary for reference in conjunction with Figure 4b, as this shows how the spectrums are compiled to create a spectrogram.

Figure 4b (Right): 3D Spectrogram Example. Shows an example of what the spectrogram would look in 3-D, rather than the 2-D representation (such as Figure 4a). We see that each of the output spectrums created by varying the time delay are compiled to create a spectrogram.

Moving onto Figure 5a and 5b, we can finally answer the question: Why is it called Frequency-Resolved Electrical Gating? This term can be broken down into two parts. The "Electrical Gating" was seen in the last paragraph, where the time-delayed secondary arm's electrical signal modulated the optical signal from the reference arm. This is called gating because an output is only produced when the pulses are overlapping, i.e. the optical signal cannot pass unless the gating signal allows it to. This mechanism is produced in part by how the modulator is biased, which will be discussed in Section 6.1. The "Frequency-Resolved" portion of the term "FREG" refers to this technique's usage of a spectrogram to characterize the input. Because these pulses are too fast to be measured with a typical electrical detector, we instead take "snapshots" or probes of the input at various positions in time. This FREG output pulse is then fed into a spectrum analyzer, which breaks down the frequency components or wavelengths which compose the signal. This deconstruction of the signal occurs via measuring the power of the constituent wavelengths in the signal, then mapping it in a power-wavelength spectrum. A spectrogram is merely a collection of spectrums, at differing time delays. An example of a spectrogram is shown in Figure 5a. This "frequency-domain" spectrogram can be deconvolved utilizing a blind deconvolution algorithm to obtain the desired pulse information. Thus, the term "frequency-resolved" extends from the fact that we are using the frequency contents of the signal to resolve, or conclude, the pulse information.



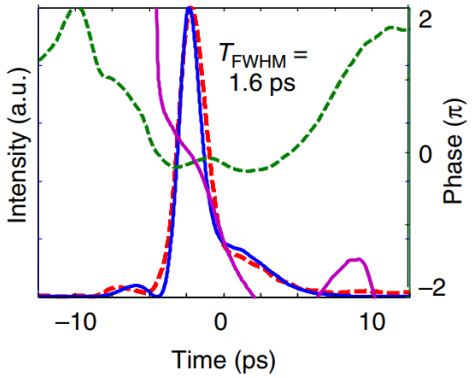




Figure 5a: 2D Spectrogram Example. Shows an example of a 2D spectrogram. These spectrograms will be the output from the spectrum analyzer and the input into the deconvolution algorithm. [3]

Figure 5b: Retrieved Pulse Phase and Amplitude. Shows an example of the retrieved pulse and phase information from a spectrogram. Ideally, our GUI will return a similar result. The dashed red line shows the measured intensity, dashed green shows the measured phase, and the magenta and blue are the respective modelled values. [3]

To reiterate, the spectrogram measured by the OSA is a measurement produced in the frequency domain. This is important, as the time-frequency relationship is the crux of what makes spectrographic techniques such as FROG and FREG so successful. We know that the time-frequency relationship for signals is inverse, meaning that signals which are short in duration (time-domain) are composed of a wide range of frequencies or are "spectrally broad" in the frequency domain, and vice-versa. Due to the ultra-short nature of the pulses used, material dispersion effects have a strong effect on pulse propagation. Dispersion is a phenomena where different wavelengths experience different velocities when propagating through a material [25]. This is because refractive index is inherently dependent on wavelength. Thus, the large span of frequencies which compose an ultra-short pulse are affected differently in terms of propagation speed, causing pulse broadening. This ties back to characterizing these optical pulses in duration and phase, as pulse broadening due to dispersion threatens the signal integrity and limits the bandwidth of data transmission systems. Once a pulse is characterized, measures can be taken to counteract these dispersion effects.

The spectrogram can be used to determine the desired optical pulse properties via blind deconvolution. One of the biggest difficulties in this set-up is that not only is the input pulse not known, but the system transfer function is also unknown. This is the type of problem blind deconvolution aims to solve. A property of linear shift invariant (LSI) systems is that if two transfer functions amongst the input, impulse response/ system and output are known, the other transfer function can be found or characterized. Another relevant property is that convolution in the time domain becomes multiplication in the frequency domain. We also know that the Fourier transform transforms a function in time into a function in frequency. Thus, typically, cumulatively we could use these properties to easily solve for either the input, output or impulse response of a system. However, as we do not know both the input and the system transfer function, we must use a more complicated algorithm to decipher the input. Blind deconvolution utilizes educated assumptions about the system's input and transfer function to recreate the output function produced from the

system. These assumptions are then iterated until the guessed input and system transfer function match the original spectrogram. This complex algorithm will be discussed further in Section 3.3.3.

The last relevant portion of this system is the electronics which connectorize all the various components and sub-systems. The objectives for the electronics include communication to the TDL, supplying power, and controlling the grating. The overall cyclical flow of the communication within the system is as follows: A user on the PC wants to start a measurement, they enter in the scan information and press a button on the GUI to begin the scan, this sends a command through the MCU to the TDL, telling it to go to the first scan position. The motorized TDL should be fast, as the maximum possible latency of the TDL is ~5 seconds. Once the TDL position is set, the MCU must then send signals to rotate the diffraction grating such that we can begin creating a spectrum of the output signal. Since the system is manual, the user will need to capture the spectrum on the oscilloscope and send it to the PC. Once this process is complete, the user can press a button on the GUI to increment the TDL and repeat the process.

Communication between the PC and TDL is necessary, such that the PC knows the delay that the delay line is set to, so it can accurately assemble the spectrogram. The PC will be receiving the pre-made spectrum of the FREG output pulse from the oscilloscope, but this spectrum does not contain the time-delay information, which is why we require the communication link. Additionally, the spectrums obtained by the oscilloscope will require information about which wavelengths it is measuring to ensure the spectrogram mapping is accurate. The wavelength output by the OSA correlates with the degree of rotation of the grating, which is a relation we can pre-characterize. Finally, the supplying of power and operating voltages to devices such as the two photodiodes and the diffraction grating's motor is desirable so we can limit the number of external connections the system has; however, it is to be determined what is practical in this regard.

**To** conclude the background, we find that the FREG is an elaborate system, with many factors to account for. However, this complexity comes with the powerful ability to characterize low-energy ultrashort input pulse trains.

# 2.3 Project Goals

## 2.3.1 Basic Goals

Basic goals are those which must be completed to create the simplest version of the FREG. Many of these are practically essential for the device to be functional.

- Create an apparatus to characterize low energy, optical pulses
- Create a GUI that begins the FREG pulse acquisition and builds a FREG spectrogram from the output power
- Program microcontroller for the FREG
- Use a program that deconvolves the FREG spectrogram
- Create PCB for external power delivery integration for the Mach-Zehnder Modulator
- Create and program a PCB to control an OSA with a resolution of at least 64 x 64

## 2.3.2 Advanced Goals

Advanced goals are the immediate possible improvements to make once the basic project goals are completed.

- Be able to resolve and characterize pico-second pulses
- Have custom housing for the apparatus
- Make the system setup simple for the user
- Have microcontroller software to decrease the amount of time it takes to create spectrogram from the pulse input
- Create additional features to FREG to include pulse data export to multiple file types
- Create a progress meter on the FREG PCB

### 2.3.3 Stretch Goals

Stretch goals are unlikely to be completed unless surprising significant advances are made quickly during project development. These are ideal changes to make if given the support of a company and given additional time to complete the project.

- Add an autocollimator to the setup for easy for easy free space to fiber transition
- Be able to resolve and characterize pulses on the order of around 100 femtoseconds
- Have a custom spectrum analyzer for the system
- Expand the GUI to be customize the resolution of the spectrogram, adjusting the OSA's motor rotation to match

## 2.4 Objectives

- Objectives are actions that can be taken to achieve goals, they specifically tell us how we will accomplish our goals. Design fiber connection lengths to minimize dispersion
- Design beam splitter power ratio to drive the EOM with the minimum amount of power necessary
- Design the pulse overlapping between the two branches of the system to produce accurate spectrograms
- Design the amount of gating which is needed to resolve the optical pulses
- Design a grating for the optical spectrum analyzer which has a high spectral resolution and the desired wavelength of 1550 nm.
- Design the photodetection setup for the OSA such that these low-energy optical signals can be captured and processed to produce a spectrogram
- Deconvolve spectrograms using Principal Components Generalized Projections algorithm
- Design and build an autocollimator
- Program a deconvolution algorithm to extract pulse duration and phase information from the spectrogram
- Develop a PCB to control the OSA; use pulse width modulation (PWM) for the motor and an analog-to-digital converter to read the PD output
- Develop a PCB to handle power distribution to components using regulators
- Build custom housing from wood

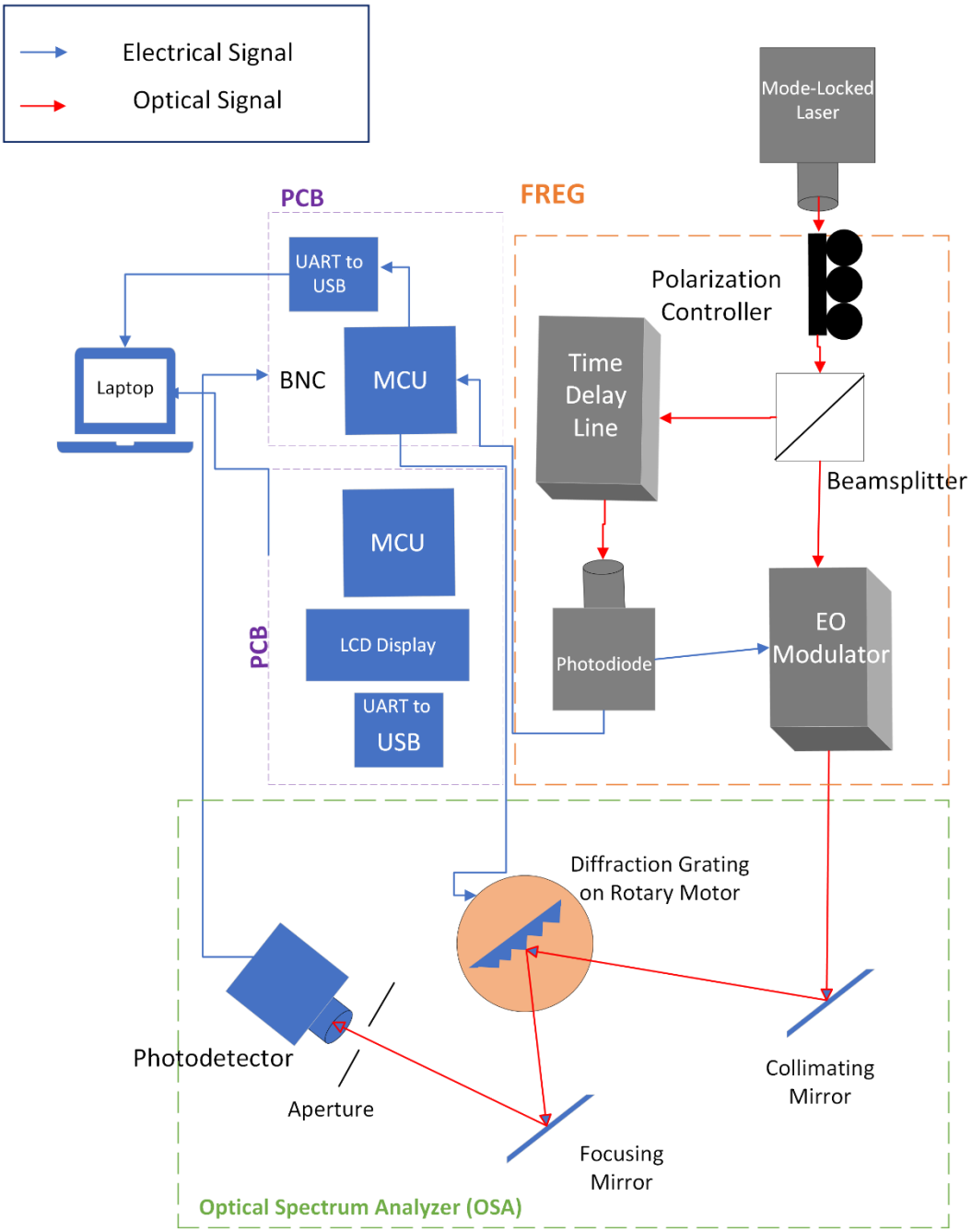



Figure 6: System Overview. Blue lines indicate electrical connections; red lines indicate optical signals.

## 2.5 Engineering Specifications

| Table 1: Engineering Specifications | | |
|---|---|---|
| # | Specification | Unit |
| 1 | Contrast of Pulse Overlapping | <5 dBm |
| 2 | OSA Motor's Angular Precision | <0.03° |
| 3 | FREG algorithm attainable accuracy (Z error) | <5*10-3 (0.5%) |
| 4 | OSA ADC Resolution | >10 mV |
| 5 | Portable Housing | ~ 2 ft x 3 ft |
| 6 | Total Pulse Retrieval Time / Full System Operation Time | < 30 minutes |
| 7 | OSA Spectral Resolution | 4-5 nm |
| 8 | OSA Spectral Bandwidth | 1515 nm – 1585 nm |
| 9 | Minimum Measurable Pulse Width | ~20 ps |
| 10 | Minimum Measurable Pulse Energy | ~40 pJ |

# 2.6 Block Diagrams

## 2.6.1 Hardware Block Diagram

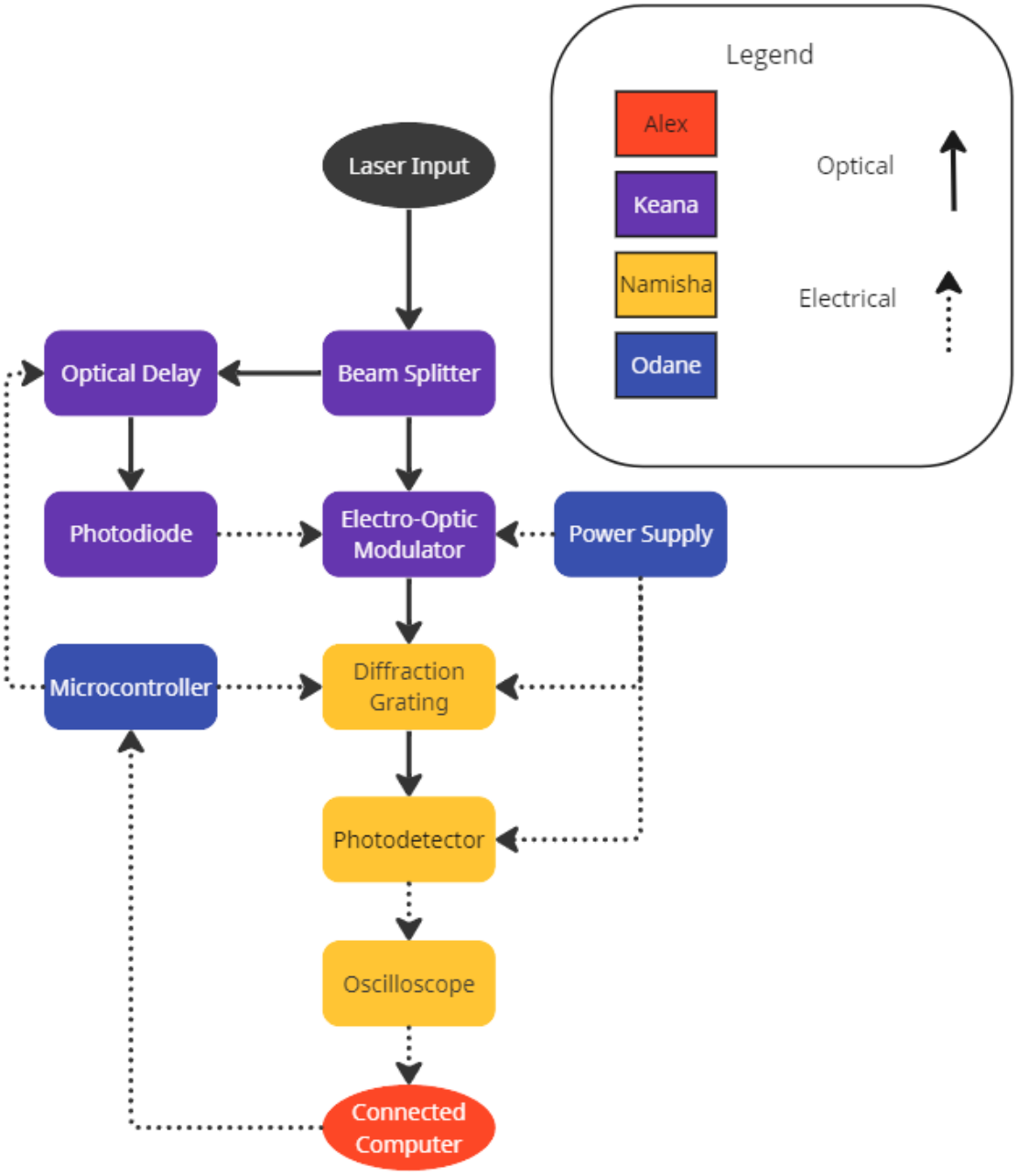



Figure 7: Initial Overall Block Diagram.

## 2.6.2 Electronics Block Diagram

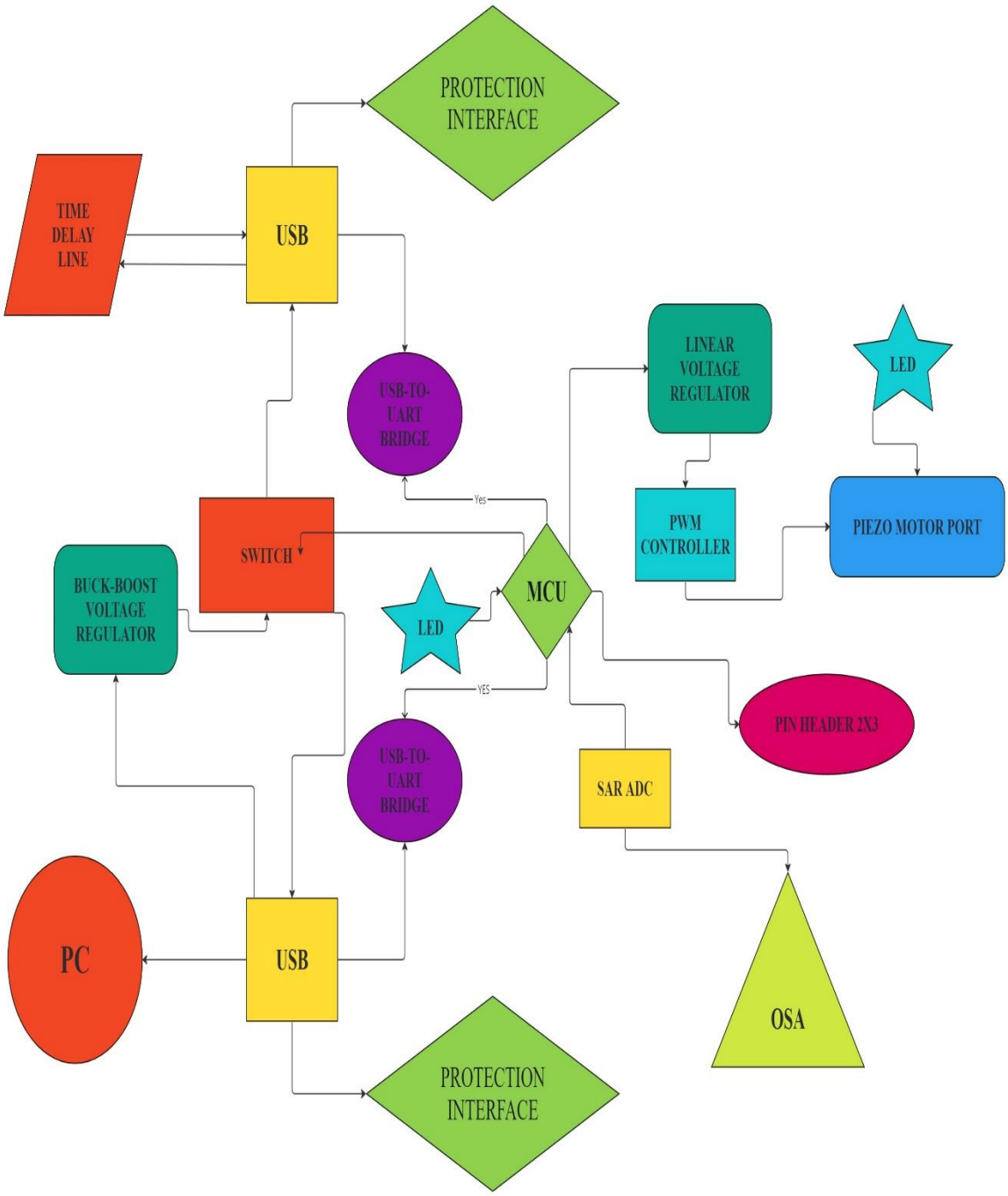



Figure 8: Initial Electronics Block Diagram.

### 2.6.3 Software Block Diagram

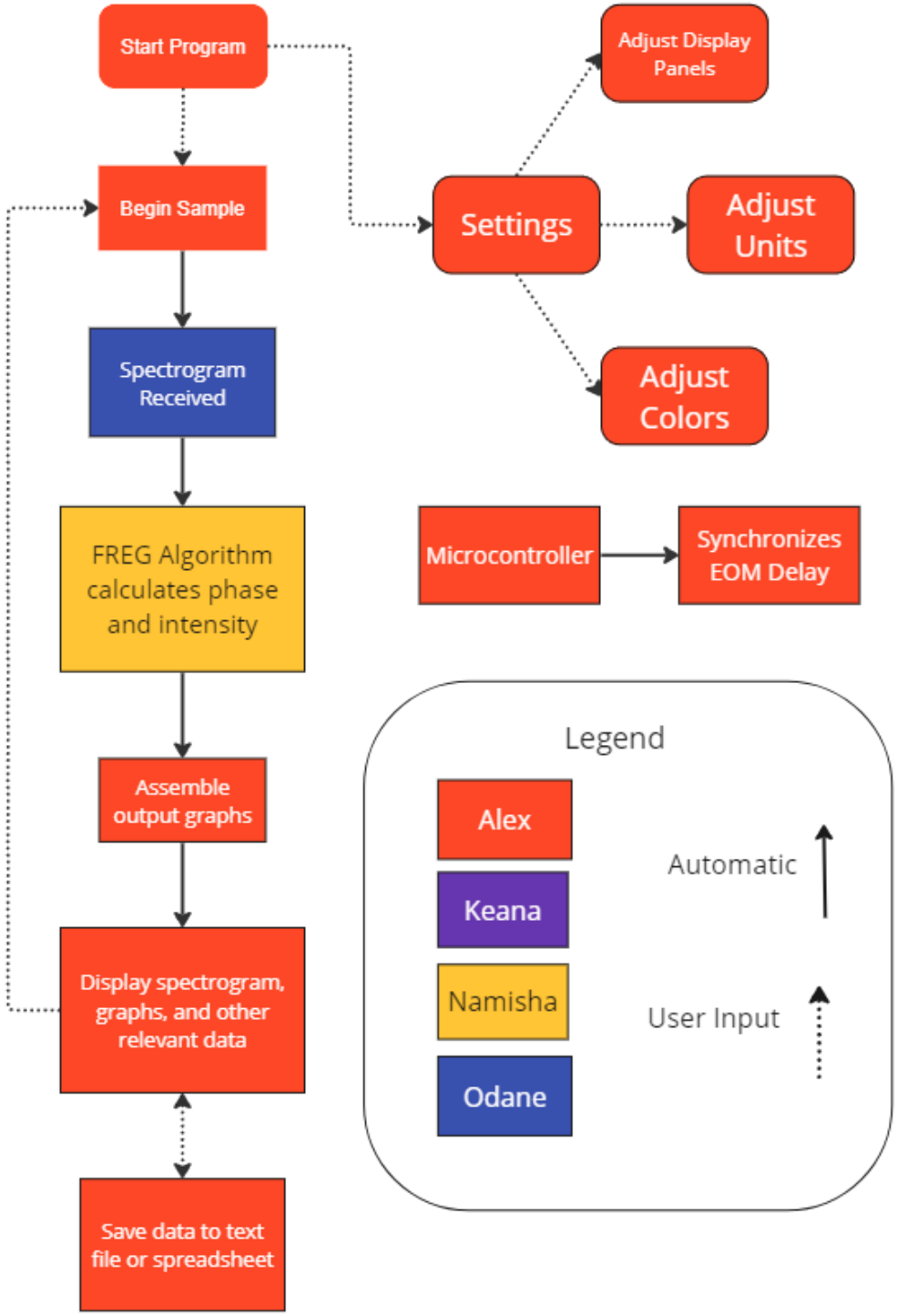



Figure 9: Initial Software Block Diagram.

# 2.7 House of Quality

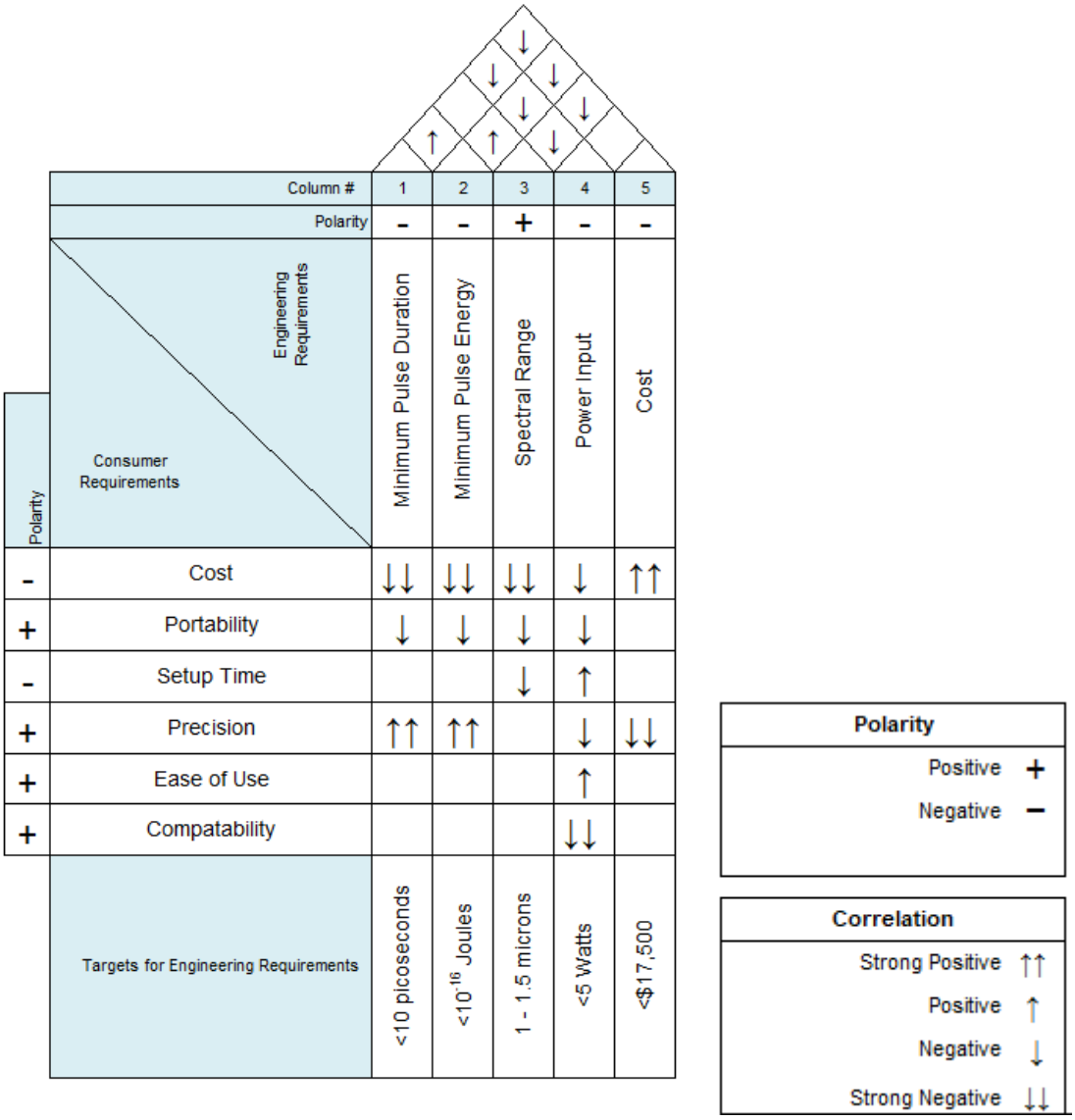



Figure 10: House of Quality for the FREG device.

## 2.7.1 House of Quality Description

The house of quality indicates that the desired outcomes of reducing the minimum possible pulse duration measurable and the minimum pulse energy measurable will decrease with cost. This means that more money will need to be spent to reach the main goal of measuring pulses with a duration of <10 picoseconds. Additionally, larger equipment has the ability to measure shorter pulses with a larger spectral range, so portability becomes more difficult as these requirements are met. Precision is the final consumer requirement with significant relation to the engineering requirements: improving the minimum pulse duration and pulse energy makes the device more precise.

The ease of use, compatibility, and setup time are more singular. The ease of use and compatibility are tied to the power input requirement due to the power input port of the FREG. If USB is used, the power input will be lower than other ports but the compatibility with computers will be higher. Using a more common cable makes the device easier to use, as a commonly used computer can be connected to the device and used rather than needing to find a computer and install drivers for a port that is not commonly used.

The roof of the house of quality shows the relationship between the engineering requirements. The minimum pulse duration has positive correlation with the minimum pulse power, as a faster modulator and photodiode will decrease the minimum values of both. However, reducing power input and cost will reduce the maximum speed of the modulator and photodiode. As minimum pulse energy decreases, the cost and power input increase for the same reasons as the pulse duration. Lastly, the spectral range decreases as cost and power decrease.

# Chapter 3 Research

## 3.1 Existing Similar Projects, Products and Relevant Technologies

The FREG has no commercially available alternatives. This is due to its relatively niche application and its configuration. Thus, there are no similar products to the system we will be building. However, there are similar projects in terms of adjacent research papers and researchers who have built systems similar to FREG. These papers will be discussed as a related work to our own work.; Specifically, we will be referencing the work of our advisor, who has built this system previously. An interesting note on the term “FREG”, is that the term was concocted by researchers who were inspired by the FROG and utilized its configuration for use in the microwave domain [4]. Our use of the term returns the application to the optical domain.

### 3.1.1 FROG

Related works to our project mainly concern the FROG and TADPOLE, the original proposal of the FREG, and more recent works utilizing the FREG. The FROG was first proposed in 1991, with a review article in 1997 solidifying its credibility as a measurement tool. The review article, “Measuring ultrashort laser pulses in the time-frequency domain using frequency-resolved optical gating”, compares several beam geometries which are each a different FROG configuration and reports the performance of the pulse retrieval from each method. As previously mentioned, FROG requires non-linear optical pulse mixing, which is inherently high-power, and does not meet our requirement of an apparatus to measure low-energy pulses. A difference between the FREG and FROG besides their set-ups is that the spectrogram of a FROG is symmetrical due to the FROG set-up. This means that the deconvolution algorithm of the FROG likely assumes symmetry in the spectrograms, and this will need to be accounted for in our code, which will reference the original FROG code [5].

### 3.1.2 TADPOLE

A system called “TADPOLE” is mentioned in the FROG review article [6] for the measurement of weak or complex pulses, which is applicable to our case. The difference between

TADPOLE and FROG is that TADPOLE combines FROG and spectral interferometry to achieve more sensitive measurements. TADPOLE sums the spectrum of two pulses, the exciting pulse and the resultant pulse, to retrieve the pulse information. Specifically, this set-up measures the strong exciting pulse to the laser source using FROG, and then uses spectrometry to deduce the weaker target pulse we are trying to characterize. This works due to the principle that any ultrashort pulse will require a high-energy input pulse to excite a non-linear medium. This means that weak pulses will always be accompanied by a high-energy exciting pulse. This is different from the FROG and FREG, which both utilize measurements of the spectrum at various time delays to extract the pulse information, as the TADPOLE only requires a single measurement of the spectrum to retrieve the desired information. However, it is not always possible to measure the exciting pulse to the laser source, which is one of the reasons why we choose to create a FREG over the TADPOLE [6].

### 3.1.3 SEA TADPOLE

Another version of the TADPOLE is the SEA TADPOLE, which uses spatial fringes instead of spectral fringes. SEA is abbreviated to mean Spatially Encoded Arrangement, while TADPOLE is the same abbreviation as stated in the previous paragraphs. This system improved the spectral resolution and gained a factor of around 5. The SEA TADPOLE was also used to measure complex pulses to achieve spectral super-resolution. This was done by measuring the spectral phase of a 14-picosecond double pulse that was generated by a Michelson interferometer. This technique is able to determine the pulse intensity and phase for long pulses that have a finer spectral structure. The flaw this SEA TADPOLE system has however is the extreme sensitivity it has due to its linear-optical method. Only a small portion of the pulse beam is needed to be coupled into the device along with polarization maintaining fibers being used to keep identical polarizations. Our system would not require the polarization maintaining fibers, however it does need to be very sensitive to capture the pulses when capturing the phases. [5]

### 3.1.4 SPIDER

There seems to be a nature trend going on because the next technique that relates to the FROG is the SPIDER, which stands for the Spectral Phase Interferometry for Direct Electric field Reconstruction. This principle is performed by combining interferometry and spectral shearing in order to retrieve the phase information. This is done without having the need to use any iterative algorithm. This method has shown higher efficiency in terms of having a faster technique to reconstruct the temporal profile of a pulse. This was shown to be beneficial for faster optimization of pulses from a femtosecond laser. These techniques also demonstrated more enhanced measurement speed and it is also able to characterize individual optical pulses. This nonlinear implementation retrieves the spectral phase by collecting and scanning the fringe pattern from the replicated pulse and the tested pulse. These were collected after going through the interferogram. A group delay is an important feature in SPIDER because once it is integrated with the frequency then the spectral phase is collected and then a Fourier transform is performed. The Fourier transform is calculated with the power spectrum to the reconstruction of the time-domain image of the electric field of the tested pulse. This relates to the FREG system as we are implementing a time delay to capture the phase of the femtosecond pulse phases by combining it with a high frequency bandwidth from a photodiode. The purpose is to also reconstruct the spectrograms from these pulses, however rather than creating an estimated image, the system is to capture the pulse durations. [7]

### 3.1.5 FREG First Configuration

The first instance of a FREG was conducted in 2002 by Christopher Dorrer and Inuk Kang [2], in the letter “Simultaneous temporal characterization of telecommunication optical pulses and modulators by use of spectrograms". They achieved a fast bit rate of around 40 Gbits per second and low peak power that was less than 1 mW. This method was also described to not rely on the need for nonlinear optics and the system is extremely sensitive, hence why it has been adopted for the purpose of low-energy characterization of 1550-nm sources for telecommunications. The main difference between this paper and our intended set-up is a higher desired operating frequency due to a shorter input pulse width, and instead of using an electro-absorption modulator as the gate, we are using an electro-optic modulator. Their set-up also tests whether amplification, broadening of the spectrum using non-linear self-phase modulation, and then linear recompression of the signal affects the retrieved pulse. They also attenuate the input signal from 0.1 mW to 0.1 μW to see how sensitive the FREG is. In both cases, the retrieved pulses are as expected, with minimal error. The acquisition time of the desired pulse information for this system was 3 minutes. However, as speed of retrieval is not one of the main priorities for our customer, we will prioritize the accuracy of the system first. However, it would be favorable to improve on this acquisition time. Thus overall, this letter not only was the first demonstration of a FREG system, but it also demonstrated robustness in operation and defines some design parameters which we utilized for our system.

For a more contemporary instance of FREG implementation, we have been referencing work by our advisor, Dr. Andrea Redondo-Blanco. Specifically, her paper called “Controlling free-carrier temporal effects in silicon by dispersion engineering”, where she details the FREG set-up which she uses for several different research papers which concern silicon photonics and solitons. In this paper, the FREG set-up is more like the version we are making when compared to the original proposal paper, with the major difference being that the DUT is after the beam splitter rather than before it. This change does not affect the overall operation of the system, as the spectrogram can still be obtained in a similar manner. Because the set-up used in this paper is more like ours than the original proposal, we utilized it as a basis for our design. The main difference between our system and this FREG is that we aim to improve the system’s minimum pulse duration, which can be measured.

As a starting point for the software, we will use code provided by the Trebino group at Georgia Tech [5], which we shall consider a related work. This code operates using a deconvolution algorithm to produce the intensity and phase by time and frequency as described above. The FROG algorithm will be replaced with one suitable for the FREG for the same purpose of measuring the characteristics of a laser pulse. MATLAB will be used to develop this algorithm due to its large libraries with math functions and due to the FROG code existing on MATLAB. The algorithm can then be included in a more complete program with a proper GUI using a language such as Java, potentially using integrated MATLAB functions.

## 3.2 Hardware Part Selection

### 3.2.1 FREG Components

For a FREG, the vital components include a photodiode, an electro-optic modulator, and a time delay line. In the following section, we will begin with an explanation of the component's function within the system, and an explanation of relevant functionality. We will then discuss the types of components which fall under the branch of the term used, why other variations of these components were not selected, and we will discuss the relevant qualities for the specific type of device we are looking for and how these qualities can affect the output. Finally, we will aggregate this information to select the final components for the project.

#### 3.2.1.1 The Modulator

The modulator is necessary to gate the pulse at different points during the pulse duration such that we can characterize the input pulse train via its impulse response. Specifically, it utilizes the output from the photodiode to modulate the input optical signal from the reference arm. This is because the signal passes through the TDL and into the photodiode and the length of the time delay or optical path length determines how much the input and delayed signals overlap within the modulator. There are a few types of basic modulators: intensity, phase, and both intensity and phase (called "I/Q").

From the general scheme of the FREG, due to our desire to measure the pulse duration and phase, we can whittle down the desired characteristics of the modulator. The set-up of the FREG is that a signal is convolved with a time-delayed version of itself to create a spectrogram. The pulse duration of an input signal is determined by multiple intensity measurements from the system using the input pulse train; however, these measurements are normalized due to the consistent "impulse" coming from the phase-delayed arm of the modulator. Thus, intensity modulation will allow us to create slices of the spectrogram via convolving the input signal at multiple points in time. We see that the spectrogram produced by the FREG is a measure of intensity, wavelength, and time.; Thus, we know that we must use an intensity modulator. Additionally, because we aim to measure pulse duration and phase, we know that using a phase modulator would only complicate extraction of the pulse phase information. For this particular spectrographic technique, we do not obtain any useful information from phase modulation, and thus, only utilize intensity modulation to extract the pulse characteristics.

There are several types of intensity modulation: Acousto-optic modulators (AOMs), Electro-optic modulators (EOMs), Electro-absorption modulators (EAOMs), semiconductor-optical-amplifier-based modulators (SOAMs), and liquid crystal modulators (LCMs) [8]. Acousto-optic modulators do not have the desired bandwidth that is expected of a system which will characterize ultrafast optical pulses.; AOMs have a <10 GHz operating bandwidth, whereas the device described in this paper has a >40 GHz bandwidth. Additionally, these bandwidths are generally "bandpass" rather than "lowpass" [8]. This makes the device operation undesirable for the FREG setup, as the characterization apparatus requires a relatively broadband response. LCMs are similarly severely limited in modulation bandwidth, due to their switching relying on the changing of its molecules' orientation, which takes milliseconds [9]. SOAMs have a better extinction ratio than AOMs and EOMs, however, the introduction of amplifier noise makes them unideal for a sensitive system. This is because noise has the potential to overhaul the signal we wish to measure because these signals are very low in energy. Additionally, they have a larger form factor, are less available, and are more costly than the typical EOM. EAOMs were used in the original proposal of the FREG [2]. EAOMs tend to have a higher modulation bandwidth and lower required drive voltage than EOMs, both of which are factors which are favorable in this set-

up. However, through our research we have found that these devices, in our desired range of 40-50 GHz, are not as readily commercially available when compared to EOMs. This could likely be due to their small form-factor which makes them more suitable for monolithic chip integration [10]. Additionally, they experience more chirp than EOMs and the amount of chirp changes with voltage [11].

With regards to EOMs, there are two main configurations: Pockel's Cell (PC) and Mach-Zehnder (MZ). The Pockel's Cell's utilizes polarization, whereas the Mach-Zehnder configuration is based on interferometry to produce an intensity modulation [10]. PC modulators utilize a bulk anisotropic crystal in a (typically) cylindrical housing, wedged between two electrodes, to modulate incoming optical signals. These devices impose a phase delay on incident optical signals when a voltage is applied to the crystal through the electrodes. Specifically, an applied voltage alters the polarization state of incident light. Thus, to use a PC for amplitude modulation, the PC must have a polarizer placed both in front of the PC and after it. This allows the modified polarization to be converted into a modulation in light intensity. This is because polarizers block light polarizations which don't align with their designed polarization state.

Pockel's cell modulators have a significantly lower bandwidth (<10 GHz) and are much bulkier in comparison to MZ modulators. In addition, a majority of Pockel's Cells are for free-space optics. This is important because we require the modulator to be fiber connectorized due to the low energy optical pulses used in the FREG. This is because waveguiding (such as optical fiber) will reduce input energy losses better than free space propagation especially if the input optical energy is uncollimated. [11]

The Mach-Zehnder modulator utilizes the two-arm interference structure of Mach-Zehnder interferometers with one important change: The optical path length (OPL) change and subsequent phase shift is induced in the device via the electro-optic effect rather than manually via mirror movement. This allows the device to be integrated and fiber connectorized rather than free space, which again reduces the optical energy losses. The linear electro-optic effect (also known as the Pockel's effect) [12] is when a voltage change induces a refractive index change in materials with a specific crystal structure. Specifically, the linear electro-optic effect shows a relation between the material polarization and the square of the applied external field [13]. Lithium Niobate ($LiNbO_3$) is one of these materials. Lithium Niobate (LN) is a very common material for photonic devices due to its strong electro-optic effect, and in this case is the material used for the MZ modulator. LN has a negative uniaxial crystalline structure, which can help in derivations of the linear electro-optic coefficients for the material. The Pockel's effect in LN can be quantized via the associated electro-optic coefficients, shown below:

Table 2: Pockel's Effect or Linear Electro-Optic Coefficients and Refractive Indices for Lithium Niobate at 1550 nm.

| r13 (pm/V) | r51 (pm/V) | r33 (pm/V) | r22 (pm/V) | no | ne |
|---|---|---|---|---|---|
| 8.6 | 28 | 30.8 | 3.4 | 2.210 | 2.138 |

Note that r42=r51, r22=r-12=r-61, r12=r23, where the electro-optic coefficients are measured in picometers per volt. These coefficients refer to the change in optical path length per voltage due to an applied electric field. These coefficients describe the directions in the lattice

geometry which contribute to this change in refractive index and their magnitude of influence. “no” and “ne” denote the ordinary and extraordinary refractive indices respectively.

The device structure of a MZM consists of the previously mentioned constituents: A 50/50 splitter, two optical waveguides in bulk lithium niobate (LN), RF waveguides and a 50/50 combiner. This structure can be seen in Figure 3 The 50/50 splitter splits the optical input in half, guiding it into each of the LN waveguides. The LN optical waveguides have a structure similar to optical fiber, where there is a higher refractive index trapping light within a medium of slightly lower refractive index. This trapping is based on a phenomenon called total internal reflection (TIR). To achieve this designed difference in refractive index for TIR of the incident light through the waveguide, Titanium doping is commonly utilized which increases the refractive index of the LN.

Thus, the light in the MZM is guided via total internal reflection, where the dimension of the doped waveguide determines the propagating light’s mode and the effective refractive index it experiences. The RF waveguide introduces a modulating signal which changes the refractive index of either one or both arms of the modulator, depending on the modulator configuration. The change in refractive index is precisely due to the movement of charge carriers within the MZM, due to the applied voltage. The refractive index change, as previously mentioned, is due to the Pockel’s effect, and is realized as a change in optical path length for the optical signal.

Both the DC bias voltage and RF bias of the modulator contribute to a relative phase difference between the two arms of the MZM. When these optical signals with a difference in phase are recombined, the output is intensity modulated accordingly. This recombination of light causing the intensity modulation is why we refer to this method as an interferometric-based modulation, compared to the polarization-dependent modulation of the PC. However, some properties of the polarization within the material do play a part in the overall functionality of this device.

Typical characteristics of the MZM we used to determine which device would be best for this set-up included the electro-optic bandwidth / S21 response, wavelength range, RF impedance matching, driving voltage, insertion loss, extinction ratio, electrical connector type, and optical connector type.

The electro-optic (EO) bandwidth tells us the range of operation for the modulator. The electro-optic bandwidth of a modulator is limited by the shortest pulse which the device material can accurately respond to. This can be thought of similarly to slew-rates in op-amps, if the input changes faster than the device is able to respond, the device will not have an output which is as sharp in slope as the input. Eventually, if the device's response rate is exceeded too much, the input pulse may not even be detectable by the device. Thus, the electro-optic response of a modulator is a measure of a device’s ability to respond to changes in an applied electric field. This applied electric field causes a change in carrier concentration within the device, which changes the refractive index, as previously mentioned.

When looking at graphs of EO bandwidth, we see that “S21” is used to describe the response. S21 refers to a signal emerging from port 2 of a device due to a stimulus from port 1 of a device, and thus represents transmission or forward power gain. This is important because we wish to maximize the response of this system and be able to modulate short optical pulses (picosecond- 100 femtosecond), which require 10+ GHz of bandwidth, at least. Generally, devices

were advertised utilizing their -3 dB and - 6 dB bandwidths. Ideally, for this system we were looking for –3 dB bandwidths of 35 GHz or larger. This generally guarantees that the device will operate up to 50 GHz as typically the roll-off of the frequency response for these MZMs are not steep.

The wavelength range is vital because we want the modulator to be able to modulate optical signals with the input wavelength we desire. This wavelength is 1550 nm and is in the C band, which is a telecommunications standard operating wavelength range which spans from 1530 – 1565 nm [14]. Modern optical fibers have the lowest losses in this wavelength range which is why a wavelength of 1550 nm has become a standard operating wavelength for optical communications.

Impedance matching is important once you reach the radio frequency, or RF, range of electrical signals. At high frequencies, electrical signals behave similarly to optical signals. For example, they experience reflections, dielectrics experience standing RF waves, they have a forwards and backwards transmission, etc. Light experiences some fraction of reflection and transmission at an interface or change in refractive index. RF signals also experience reflection and transmission at interfaces, where rather than comparing the refractive index, we look more to the property of characteristic impedance, to identify how the RF wave will be reflected and transmitted through the coaxial connection. Thus, we prefer for the impedance between RF transmission lines or waveguides to be matched to minimize losses due to reflections away from the desired signal direction.

The driving voltage of an MZM is what typically controls the phase shift in each of the arms of the device. As previously mentioned with the electro-optic effect, it requires an applied electric field to change the refractive index, and thus the OPL, of light going through a material with strong electro-optic properties. The driving voltage is typically externally applied with the use of a modulator driver. However, due to a combination of the type of modulator we have chosen and the configuration of the FREG, this is unnecessary. There are two types of MZMs when it comes to the type of drive: single drive and dual drive. A single drive means that only one of the arms of the modulator is being biased with a voltage. Thus, because we have chosen a single drive, and have the photodiode linked up to the MZM, the photodiode replaces the need for a modulator driver.

Furthermore, single drive means that the full driving voltage must be applied to the arm to get the maximum extinction ratio [15]. The driving voltage or wave voltage is often denoted as $V\pi$ and refers to it being the voltage required to induce a phase shift of $\pi$ in the output signal. In dual drive, both arms are being driven, and only half of the driving voltage needs to be applied to each to achieve the maximum extinction ratio. By making these applied driving voltages equal in amplitude and opposite in sign, chirp can be eliminated from the modulator. Thus, we see that dual-drive is preferred over single-drive modulators, as chirp is an undesirable quality.

Elimination of chirp in the FREG is important for preserving the integrity of the measured optical pulse information, specifically the measured phase information. This is because phase shows how the frequency components in a signal change over time, and chirp is either the increase or decrease of a signal's frequency over time. Chirp is often due to nonlinearities in a material or dispersion [16]. Chirp and the types of drives in MZ modulators link further to the types of device geometries and the crystal cuts within MZ modulators.

Due to biasing, dual drive MZMs are inherently symmetrical in structure which eliminates chirp. However, for single drive MZ modulators, there is the Z-cut configuration and an X-cut configuration, which each refer to the crystal cut of the MZM which subsequently creates the device's geometries. X-cut is preferable to Z-cut single drive MZM modulators because they are more symmetric and consequently chirp-free [17].

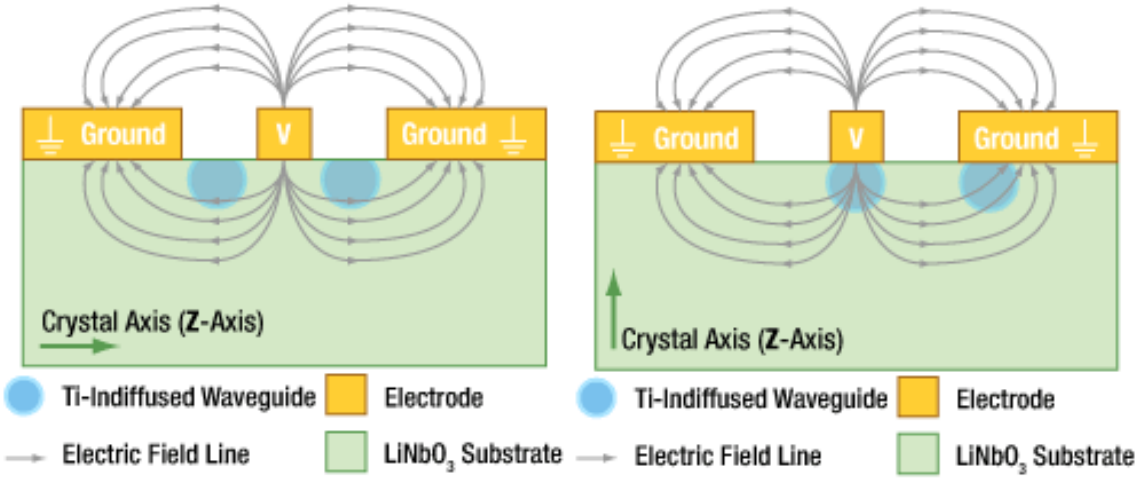



Figure 11: MZM Crystal Cuts. Shows the differences between the different single-drive MZM crystal-cut configurations. [17]

Insertion loss is a measure of the signal power loss in decibels when a signal travels into a given device. Due to the low-energy application of the FREG, we must be extremely cautious when factoring the signal losses. Losses in this set-up will likely be mainly attributed to insertion losses into various components and fiber propagation. Thus, these values must be taken into account to make sure that they do not exceed nor eclipse the desired signal strength.

The extinction ratio is essentially the contrast, or maximum output to minimum output you can get out of a device. This extinction ratio relates to establishing the gating of the FREG. As previously mentioned, the extinction ratio must be designed for via the modulator biasing, specifically the DC biasing. In Section 6.1, we will discuss why we have biased the modulator the way we have and how we characterized the extinction ratios of our modulators. Overall, the larger the extinction ratio is, the better it is for the device operation.

The electrical connection of note with the MZ modulator is the RF connector, as this is highly specific and is engineered to minimize losses by guiding the RF signals. Typical RF connectors encountered with the MZ modulators tended to be V- and K- connectors, or 1.85 mm and 2.92 mm connectors, where 1.85 mm and 2.92 mm designations refer to the diameter of the outer conductor of each connector. These connectors are designed to operate mode-free up to 65 GHz and 40 GHz respectively. Another common MZ modulator RF connector is the GPPO, which has a cutoff frequency of 65 GHz and a smaller form factor than V- and K- connectors. Multimode RF signal propagation occurs above the cut-off/mode-free frequencies specified. Thus, being aware of the connectors past their mechanical properties is important to maintain signal integrity, especially since our stretch goal is to operate at or above 50 GHz. Additionally, connector matching and being aware of the types of RF connectors is necessary because changing waveguides, which in the case means transferring from one type of connector to another, causes signal losses.

Finally, we want our optical connections throughout the system to be matched, and we also want to minimize the number of optical connections made throughout the system. Both of these factors are important for minimizing optical losses, because at each discontinuity point there will inherently be a loss of signal. This is because no connection, whether it be a fiber splice or connector, will be as low loss as a continuous waveguide. Matching optical connections simply refers to optical fiber connectors, for example Flat Connectors (FC), Angled Connectors (AC), and Polished Connectors (PC). It is already standard in the fiber-optics field that different connectors are not connectorized without a patch chord which transitions between the two. This is especially important in our system due to the low-energy nature of the set-up and concerns about sending high-power reflections back to the laser source.

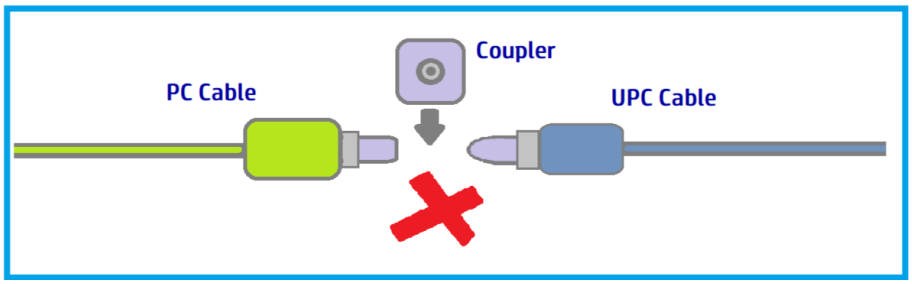



Figure 12A: Shows the proper connectorization of fiber to minimize back reflections and insertion loss. Fig. 12A demonstrates that the coupler cannot be used because the PC cable does not match the patch cord.

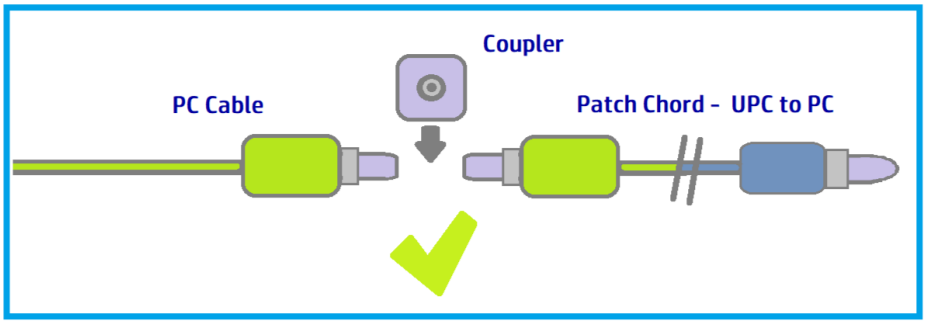



Fig. 12B correctly shows the fiber ends must be the same to use the coupler properly.

We now come to the comparison of the components, as shown below in Table 3. We have additionally added cost to this analysis along with the previously mentioned factors, as we have to keep the system reasonably priced for the consumer. We have neglected showing the wavelength range, impedance matching, and optical connectors as these are consistent between all of the options.

We have found through our research that these bulk MZMs have become relatively sparse on the market, as the research and market desires for MZMs have pushed towards integrated thin-film modulators and more complex MZMs (such as quad-MZMs). This is because there was a large shift away from these devices due to changes in the telecommunications domain. The integrated thin-film MZMs are used in applications such as photonic integrated circuits and are based on Thin Film Lithium Niobate (TFLN) technologies. The impact this has had on our project is that it was more difficult to find two-arm MZMs which were at or above 50 GHz in operating frequency, as breaching this soft limit on modulator bandwidths is only useful in niche applications

such as the creation of the FREG. TFLN MZMs currently reach operating frequencies well above 100 GHz [18]. An example we came across of this drop-off in research for better performance in these bulk MZMs is that the mentioned Fujitsu modulator in the table below with a 40 GHz operating frequency was released in 2003, and the company has not released any better performing MZMs since around that time. There are many papers that also show this trend. This demonstrates that for the last 2 decades; improvement of the operating bandwidth and overall performance of these devices has been stagnant.

| Table 3: Comparison of Mach-Zender Modulators | | | |
|---|---|---|---|
| Model No. | FTM7937EZ | IML-1550-40-G | MXAN-LN-40-PD-P-P-FA-FA |
| Company | Fujitsu | Optilab | IXBlue |
| -3 dB EO BW (GHz) | 37 | 30 | 40 |
| -6 dB EO BW (GHz) | 50 | 40 | 50 |
| Drive Voltage (V) | 1.8 | 2.0 | 8 |
| Drive Type | Dual | Single, X Cut | Single, X-Cut |
| Insertion Loss (dB) | <10 | 5 | 3.5 |
| Extinction Ratio (dB) | > 20 | 23 | 25 |
| RF Electrical Connector | - | GPPO | V, Female |
| Lead Time | In Stock | In Stock | 6-8 Weeks |
| Cost | $899 | $2995 | $5000 |

Reviewing the options for MZMs, it appears the Fujitsu modulator is the ideal option. This modulator was used in a previous FREG set-up, and since we wanted to improve the operating bandwidth of this FREG compared to previous iterations, we searched for other options. However, after researching the market, our best options still only barely scratch the 50 GHz range. The –6 dB bandwidth is significant because this is where the input is attenuated to 25% of the incident power, which means that though the device is technically still operating in the desired regime, it is severely limited. The only options which operate up to the desired 50 GHz frequency are the IXBlue and Fujitsu modulators. However, the cost of the IXBlue modulator is more than 5x the Fujitsu modulator, with its only major improvement in performance being its insertion loss, which is 35% less than the Fujitsu modulator. Additionally, its lead time is 1-2 months, which is not ideal for our current timeline. Looking at the Optilab device for an alternative, we find that it is again comparable to Fujitsu's specs, except that its cost is 3x higher and its bandwidth is 20% smaller. Therefore, we will use the Fujitsu FTM7937EZ or a comparable model for the final FREG setup.

#### 3.2.1.2 The Photodiode

A photodiode takes an input optical energy and outputs an electrical signal. For the FREG, the photodiode converts the time-delayed portion of the optical signal into an electrical signal which is used to modulate the reference arm optical signal within the modulator. Photodiodes fall under the wider category of photodetectors, which also include photoconductors, phototransistors, and photoresistors, which each detect electromagnetic radiation. All photodetector devices operate on the principle of a semiconductor absorbing region, which absorbs photons from an incident optical energy source.; This energy promotes electrons in the material from the valence band into

the conduction band, creating free electrons which contribute to a photocurrent in the device. A photocurrent is a current due to optical absorption and has the same characteristics as a normal current.

The differences between the various photodetector devices are their structures. A photoconductor consists of an intrinsic semiconductor, which has low conductivity. When a voltage is applied to this device, then and only then can incident photons be converted into a usable photocurrent. A transimpedance amplifier can be used to convert the photocurrent into a usable voltage in the overall system. The signal through a photoconductor experiences gain when in the operating region. Photoconductor structure typically consists of an intrinsic semiconductor with metal contacts. To achieve a photocurrent, the applied voltage to the electrodes of the device must be large enough to overcome the recombination time of the carriers. This voltage can be optimized via minimizing the distance between the electrodes. However, minimizing the spacing between the electrodes decreases the active region of the device, thus it is a trade-off. Photoresistors are similar to photoconductors in operation, however the largest difference is that photoconductors are active devices whereas photoresistors are passive. This means that photoresistors do not experience gain. Photoresistors are devices whose resistance decreases with an increase in input optical energy, similar to photoconductors. Photoresistor structure typically consists of an active semiconductor layer (such as n- doped semiconductor), a semi-insulating substrate, and metal contacts.

Alternatively, the photodiode structure consists of a semiconductor junction. Photodiodes can be operated in two modes: Photovoltaic and Photoconductive. Photovoltaic operation occurs when no biasing voltage is applied to the photodiode. Despite this, it still has a high electric field in the depletion region, and thus can produce a photocurrent when connected to a high-impedance load. The photoconductive mode for photodiode operation requires a reverse biasing voltage. The reverse biasing voltage increases the width of the depletion region, which is also the active region of the device where the photon absorption occurs. This means that the quantum efficiency of the device is increased. The reverse biasing voltage also increases the drift of carriers, meaning that the device response time increases.

There are a few typical configurations of photodiodes: PN, PIN, and avalanche photodiodes. PN and PIN refer to semiconductor doping, where P- refers to p-type, I- refers to intrinsic doping, and N- refers to n-type doping. PIN photodiodes are an improvement over PN junction photodiodes in terms of efficiency because the device structure inherently widens the depletion/active region of the device via the intrinsic region. However, there exists a trade-off between high-frequency response of photodiodes and the depletion width of a device, due to carrier transit time within the device. The carriers must reach the electrodes to produce a photocurrent, however, if the switching of the input signal is too fast the generated carriers will not be able to travel to the electrodes in time. Thus, it is advantageous to minimize the depletion width if a high-frequency response is needed, making PN junctions advantageous in some cases.

Avalanche photodiodes typically have a n+-p-i-p+ structure. This structure allows for a high-amplitude electric field to exist in the p-region, which causes impact ionization. Impact ionization is when carriers with high momentum transfer their energy or cause other carriers to gain energy via dislodging them from the lattice structure. Impact ionization can be thought of as an escalating process, which can then lead to avalanche breakdown. A device is experiencing the avalanche effect if more than one electron-hole-pair (EHP) can be generated from an incident

photon, which in turn leads to the multiplication or amplification of the photocurrent. The avalanche effect occurs only under a high reverse-bias voltage. Avalanche photodiodes have the advantage of a high responsivity over other photodiode configurations [19].

In addition to the previously mentioned carrier transit time limiting the input signal frequency, there are further electrical limitations with regards to parasitic RC behavior in all types of photodiodes. Parasitic resistances and capacitances cause noise and unwanted signal oscillations in the photodiode output. [20]

Comparing the different types of photodetectors, photodiodes are typically better for detection of power in the milliwatt range, whereas photoconductors have characteristics which are suitable for optical power in the watt range [21]. Thus, because the FREG requires the detection of low-energy optical pulses with a peak optical pulse power in the milliwatt range, it would be better to use a photodiode. Additionally, due to avalanche photodiodes' high-speed, internal gain, and sensitivity, an avalanche photodiode would be preferred over other photodiode configurations.

All of the photodiodes we will be comparing are based on an alloy called Indium Gallium Arsenide or InGaAs on an Indium Phosphide or InP substrate. This structure is the most common for photodiodes in the near- to mid- infrared region due to its absorption spectrum for these wavelengths. This means that this material absorbs the energy of the photons with the wavelengths in the near- to mid- IR range well. This in turn means that the absorbed energy is more likely to promote an electron from the valence band to becoming a free carrier, which can conduct electricity and produce a current.

Typical characteristics of the photodiode used to determine whether it was suitable for the FREG setup include the electro-optic bandwidth, responsivity, conversion gain, NEP, optical return loss, dark current, reverse termination impedance, average optical input power, bias voltage, polarization dependent losses, and the electrical output connector. The bandwidth, reverse termination impedance / impedance matching, and electrical output connector are the same metrics from the MZ modulator; thus, we will not repeat their descriptions.

For photodiodes, responsivity is a measure of the electrical output per optical input. It is measured in amperes per watt (optical). We want the responsivity of the photodiode to be high, as it allows us to more precisely bias the MZM. This characteristic is dependent on the absorption of the semiconductor materials in the device and their quantum efficiency, which are both material properties. [22]

Conversion gain is another characteristic of photodiode performance which is like responsivity. The conversion gain of a photodiode is the ratio of the output power to the input power. Thus, for signals which are undesirably weak, the conversion gain's inherent amplification during the conversion of the energy from optical to electrical may be useful.

In photodiodes, there is a trade-off between bandwidth and sensitivity [23]. This is because, for a detector to be highly sensitive, it must have the ability to detect weak signals. However, this requires a large absorption area, which decreases the bandwidth via increasing the transit time of carriers.

The NEP refers to the noise equivalent power. This parameter quantifies the sensitivity of a sensor. It is defined as the noise-power for the target bandwidth of a system or the noise spectral

density. It will help us in determining whether the beam-splitter power ratio is sufficient to overcome noise and losses in the system.

The dark current of a photodetector is a measure of the electrical current produced when there is no incident light on the sensor. It is considered a form of noise but can easily be measured and accounted for in calculations, since it is a constant value.

The optical return loss of the photodiode is a measure of how much signal is reflected out of the system and is analogous to the S11 parameter. We ideally want this value to be 40-60 dB, which means that the return loss is a small value. The insertion loss is analogous to the S21 parameter, and we want this value to be small as it indicates how much power is delivered to the output port of the device.

Table 4: Comparison of Photodiodes

| Model No. | XPDV2320R | PQS40A-L | DX50AF |
|---|---|---|---|
| Company | Finisar | Albis | Thorlabs |
| -3 dB EO Bandwidth (GHz) | 50 | 40 | 50 |
| Responsivity (A/W) | 0.65 | 0.80 | 0.7 |
| Electrical Connector | V, Female or Male | K, 2.92 mm | V, Female |
| Cost | $4000-$5000 | $3880 | $5775 |

We will prioritize the electrical connector and responsivity of the photodiode. This is because the RF electrical connectors are expensive, and we want to minimize these costs as much as possible by working with what we have. The responsivity of the photodiode is our other priority mainly because it will be one of the heaviest influences on how much optical power will need to go through the secondary arm of the FREG to bias the EOM. Like the EOM, the device bandwidth is vital, as ideally the PD bandwidth would match the modulator bandwidth, since it is driving the modulator. Since all of the listed PDs are in the 40-50 GHz range, this does not narrow down which PD should be chosen. Thus overall, we find the PQS40A-L to be the top choice due to its high responsivity and low cost, followed by the XPDV2320R.

#### 3.2.1.3 The Time-Delay Line

The time delay line is necessary to produce the shifting of the gate function, which will contribute to the production of the spectrogram. The time delay line takes the minority of the optical power from the beam splitter and passes this optical signal through an extended optical path, which causes the signal to lag in time in comparison to the reference arm (which includes the modulator). This lagged signal is then combined with the non-lagged signal in the electro-optic modulator, which produces an intensity modulation. By repeating this process with different time-delays we can produce the spectrogram.

Typical characteristics of the time delay line which will affect FREG project are the delay line's configuration, the delay range, insertion loss, delay resolution/ step size, consistency, speed, and precision. Types of common time delay lines include piezo-transducer, piezo-electric motorized, fiber-optic, free-space motorized, free-space manual, and rotary. There are also dispersive delay lines, however these are undesirable as we wish to avoid dispersion of the input signal. The size of the time delay needed will determine the type of time delay line used in a system. For scenarios of electro-optic sampling, such as with the FREG, a large time delay is often required. In our case, we are taking a measurement from a train of optical pulses, and thus, the delay must extend further than a simple change in the phase of the signal. We know that any delay-line which relies on piezo-electric effects will be unideal as the induced optical path length change in these materials tends to be on the order of microns to nanometers. For our set-up, a maximum delay of 330 picoseconds is sufficient. This value, assuming the light is travelling through air mostly equates to approximately 99 mm or ~10 cm. These lengths can primarily be achieved using a motor-driven change in optical path length. We opt for motor driven over a manual stage set-up for precision. A fiber based TDL would be another potential option because it could provide the optical delay we are looking for; however, it does not allow for the precise tuning in delay duration that we would need. This is because fiber-based TDL's are generally configured as a set of fiber loops, where the delay range is created by connecting the loops together. Thus, there is a certain coarseness to the delay duration which motor-driven devices overcome, given their motors have a fine step size. The disadvantage of motor-driven TDLs in comparison to fiber-based TDLs is that systems which are more mechanical in nature, such as the motor-driven device, are likely to lose their reliability over-time much more quickly.

Vibrations in the system during adjustment of the time-delay line is not a concern, as the measurement of the convolved pulse intensity is measured after the time-delay line adjustment. The vibration is only a limiting factor to the speed of the measurement and production of the spectrogram.

Table 5: Comparison of Time-Delay Lines

| Model No. | MDL-002 | MDTD-01C111313 | Uniphase HD3 |
|---|---|---|---|
| Company | General Photonics | Agiltron | JDS |
| Insertion Loss (dB) | 1.3 | 1.6 | TBD |
| PDL (dB) | 0.1 | 0.2 | TBD |
| Return Loss (dB) | 50 | 55 | TBD |
| OPL (up to ps) | 330 | 330 | 170 |
| OD resolution (fs) | 1 | 1 | 20 |
| Cost | $3870 | $2230 | $3098 |
| Lead Time ARO | 4 Weeks | 3 Weeks | None |

Overall, due to the similar specifications between the Agiltron and General Photonics TDLs, we decided to order the Agiltron TDL due to its shorter lead time and cheaper price. An increased insertion loss of 0.3 dB but +5 dB better return loss was enough to consider the TDLs relatively equal in specifications. Regardless, for our purposes, 0.3 dB (or ~5% IL difference) was not significant enough to sway our decision, especially with a price difference of over $1k.

#### 3.2.1.4 Additional FREG Components

#### 3.2.1.4.1 Beamsplitter

The beamsplitter is the starting point of the FREG device, as it splits the optical input power between the two arms of the FREG. As with all components in the FREG, we desire to minimize losses, especially since the typical input into the device will be low-energy pulses.

Types of beam splitters include free-space and fiber-optic. Due to the integrated nature of the FREG and the desire for low-loss of the input signal, we will be focusing on fiber-optic beamsplitters. In this category, there are FBT splitters, PLC splitters, and balanced splitters. Additionally, there are polarized and non-polarized maintained splitters.

Fused Biconical Splitters (FBT) split light from one fiber into multiple output optical fibers, or it can combine light from two optical fibers into one. This beamsplitter is fabricated by gathering two or more pieces of fibers, which are then fused onto a taper fiber device. The fibers are drawn out to the desired length to the output arm and the ratio with one of the arms be separated as the input arm. The typical wavelength the FBT is operated in is around 1310 nm to 1550 nm in most standards, but it is also able to function in the 850 nm wavelength range. The Power ratios between the two output arms can be customized to the desired power separations. The type of fiber is the beginning part of the selection process and then the fibers are tapered together into the 2x1 layout. The two fibers are the split power arms that can have a ratio of 50:50 power distribution or 90:10, etc. This splitter is well-known in industry because it is accessible to produce and the most cost efficient to manufacture.

There are disadvantages of using the FBT as well, even as the most common device. While the operating wavelength of the system is 1310 nm, 850 nm, or 1550 nm, those are the only wavelengths the FBT is able to function in. This restriction limits the FBT from operating in any other wavelength range, thus cannot be catered to niche devices. The power ratio split may experience transmission loss due to the distance and the discrepancies between the two fibers. There is no guarantees there will be exact ratio splitting between the fibers, which goes to another issue of where the power is distributing and how much is being lost to either dispersion or traveling beam going through the wrong arm. The insertion loss must also be taken into account, especially for the FBT because the device is sensitive to higher temperatures. The temperature range for the FBT is around 23º F to 167º F, anything out of that range can effect the insertion loss of the device. If the FBT is handled improperly or affected by the high temperatures, then the device ultimately fails. This would call for replacing the whole device again in order to ensure the power ratio is characterized to the proper splitting. Larger ratio splits, for example, anything larger than 1:8, the beamsplitter becomes unreliable and the stability cannot be sustained.

Planar Lightwave Circuit (PLC) splitters split light evenly throughout a single-mode operating window range of 1260 nm to 1650 nm. The splitter is able to be set up in 1x4 up to 2x32 splits of input to output optical fibers. In the fabrication process, there is one optical chip and several optical arrays in the system. The number of optical arrays is dependent on the output ratio, which the arrays are then coupled on both ends of the optical chip.

However, the potential transition from free-space to the fiber-based beam-splitter if this characterization device is not used with a fiber laser, proves a point of great losses if not engineered properly.

The decision of the beamsplitter mainly hinged upon finding a device with our calculated power-ratio with a low insertion loss and high-return loss. This process also involves characterizing the beam splitter that is chosen for the set-up, due to the inherent deviations from the ideal parameters mentioned in the data sheet. We need to ensure that these deviations will not affect our system's performance, as we desire robustness. We will discuss this beam-splitter power ratio design further in Section 6.1.

#### 3.2.1.4.2 Polarization Controller

A polarization controller is necessary in the case that there is a polarized maintained component in the set-up. Generally, Mach Zehnder modulators are designed to be polarized-maintained in input, if not in input and output. This is related to the crystal excitation within these integrated modulating devices. Mach-Zehnder modulators are typically lithium niobate based, which has a crystalline structure which attenuates the amplitude of light which does not align properly with the fast-axis of the material.

In our system, since maintenance of polarization is not necessary for our measurements, we opted for a modulator without a polarized maintained output. However, the PM input cannot be avoided, which is why the polarization controller is necessary. The polarization controller was placed between the fiber laser and the beam splitter for the demo. However, it ideally should be placed directly before the modulator. This is because none of the fiber throughout the system is polarization maintained except for the input to the modulator. This means that the polarization changes as it propagates through the single mode fiber, making the polarization less optimized. Each of the fiber-based components, which are the majority in this set-up, experiences a polarization-dependent loss. Additionally, any movement of the fibers in the set-up post-optimization could shift the polarization of the propagating optical system, making the system un-optimized. This highlights the importance of PM fiber in systems where polarization affects the output signal. For our system, we utilized a polarization controller already purchased in the lab. There was not a large concern about the specifications of this device, however for future design it will be necessary to take note of the insertion loss of the polarization controller.

The polarization controller has a total length of 5 meters, which was enough to elongate the signal.

#### 3.2.1.4.3 Fiber

Optical fibers will be used to propagate the signal throughout our system. When choosing the type of fiber that will be used for the final product, different criteria must be met. There are many types of fibers such as graded or step index fibers. There is also polarization maintaining fiber with different stress rods. These fibers have a thin glass tube in the middle that makes up the core, then the cladding is layered over the core. The cladding is usually made of highly pure silica due to the fact it is the best at transmitting light. The light travels through the core by bouncing on the inside. The cladding will block the light from escaping the core, which is known as total internal reflection. Finally, the coating is added over the cladding to protect everything inside. Sometimes a secondary coating is added for extra protection from outside forces or any form of moisture from leaking in. We must take into account how dispersion occurs when selecting the type of fiber that is to be used for the project, along with how long the fiber must be.

There are two types of fibers in terms of number of cores. The first will be the single-mode fiber, SMF, which as the name describes, has a single core at 9 um in diameter and 125 um in diameter for the cladding. SMFs are normally used for long-distance data transmission because the design minimizes modal dispersion from occurring due to its small size. The project requires significantly higher bandwidth due to the speed we will be reaching, which is a benefit the SMF has along with very low signal attenuation. There are different variations of the SMF depending on what regions or signals are desired to be optimized.

Non-dispersion-shifted fibers are optical fibers that are specifically designed to minimize the effects of dispersion in optical signals. The most common type of dispersion this fiber is designed to adjust is chromatic dispersion, which is when various wavelengths travel at different speeds through an optical medium. The optical pulses begin to lose their shape and disperse over a certain distance over time, which leads to the signal degrade. With the Non-dispersion shifted fiber, the transmission of high-speed data can travel significantly further than that of a single-mode fiber without having the signal being altered from chromatic dispersion. While the fiber cannot completely diminish dispersion, this design is best suited for long-distance telecommunications, but not for our project.

Dispersion-shifted fibers is an optical fiber that is limited but optimized to function at 1550 nm wavelength. This limitation makes it difficult to use for a variety of applications, which leads to another type of dispersion-shifted fiber for non-zero dispersion. This fiber has less dispersion than the one that is optimized for 1550 nm and is most useful for higher data-rate Dense Wavelength Division Multiplexing [25].

Another type of fiber is the multimode fiber, MMF, which has a larger core than the SMF and enables multiple cores to be in the fiber. The core sizes for MMF tend to range between 50 to 62 µm in diameter. Due to the larger core size for the multimode fiber, this causes more modal dispersion to occur over a long distance. For this reason, the fiber lengths tend to stay on the shorter end to limit the dispersion from happening. For multimode fibers, there are two common types used to this day.

The graded index fiber, which has the core is set up for the refractive index to gradually decrease towards the edges of the fiber (Figure 13). The design of the graded index fiber is rounded, which minimizes modal dispersion because the light travels in a smoother path through the core. The fiber in this case would be best in high-speed data transmissions over a short distance without needing to correct the signal.

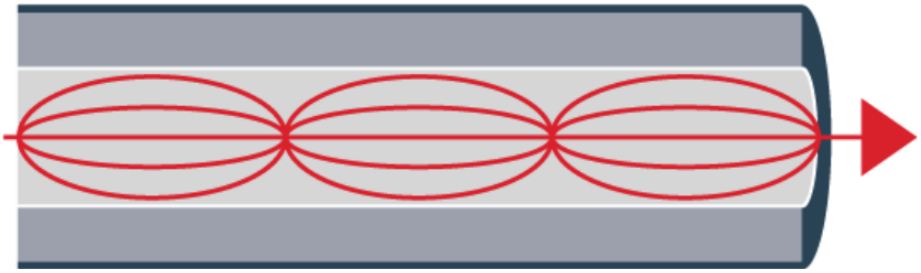


Figure 13: Graded Index Fiber with light propagating from core to edge of cladding.

The step index fiber is different from the graded index fiber because the light gradually leaves the center towards the edge of the core, the refractive index stays the same throughout the whole fiber. The images below visually demonstrate the difference in how the light behaves between the two fibers. When dispersion is not the concern for an application is when these types of fibers are typically used. The core is the same throughout the fiber without any gradual changes, which is affected by the modal dispersion.

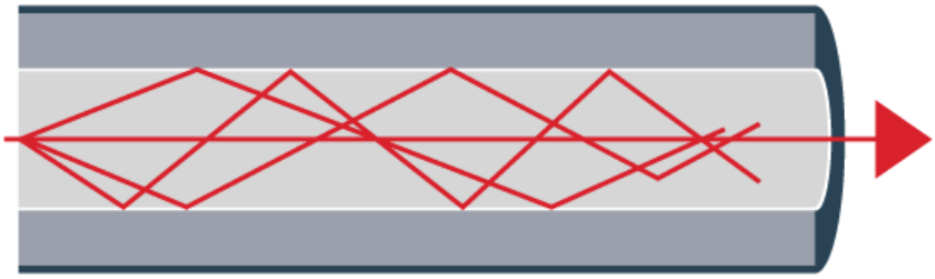


Figure 14: Step Index Fiber with light traveling in zigzag due to light arriving at different times.

Polarization maintaining fibers are very different from the previously mentioned optical fibers because this fiber requires stress member rods to be parallel to the core. This optical fiber is engineered to maintain the polarization state of the light as it travels through the core, which is done from the stress member rods inside of the cladding. These fibers are used when polarization must be maintained throughout the whole system, especially those that require extreme precision and various sensors. There are two different types of PM fibers known as PANDA and Bow-tie fibers (Figure 15). Panda fibers utilize two cylindrical rods that are parallel to the core while the bow-tie fiber has trapezoidal prisms parallel to the core. The applications of these fibers are interchangeable, but the PANDA fiber is most used because of the simpler design.

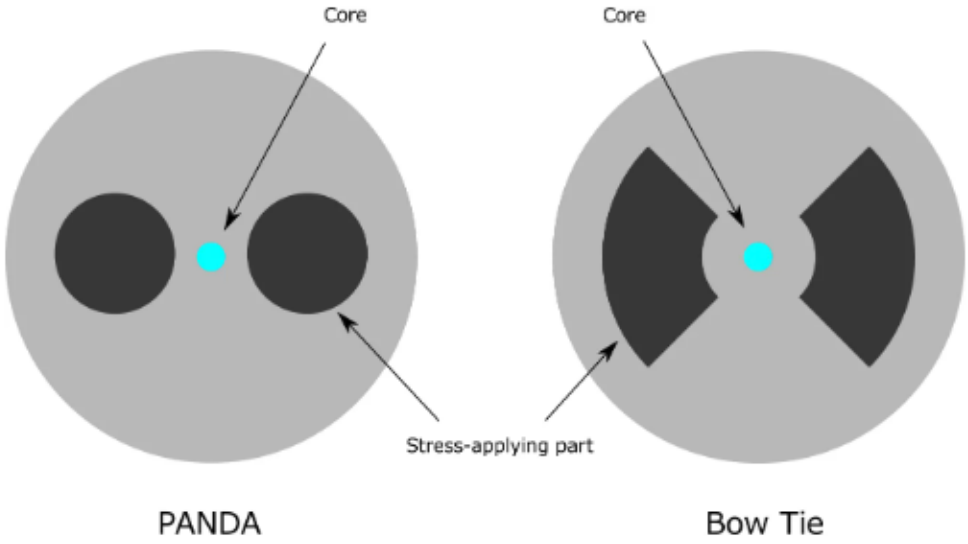


Figure 15: Schematic of two different types of PM fibers. The PANDA on the left side will be the structure of the MZM fiber input, which is different from the Bow Tie structure on the right side.

Overall, for the FREG system the single mode fiber was chosen out of all of the optical fibers because of the limited dispersion that occurs in the SMF. The input fiber of the modulator that was used for the first optical demonstration was a PANDA polarization maintaining fiber, which lead to the discussion of whether to keep the system polarization maintained or to switch back to the scrambled signal. In this case for the modulator, we will be using a PANDA fiber to connect the input fiber of the laser to the input fiber of the modulator. The rest of the setup however was decided to keep using the single-mode fiber.

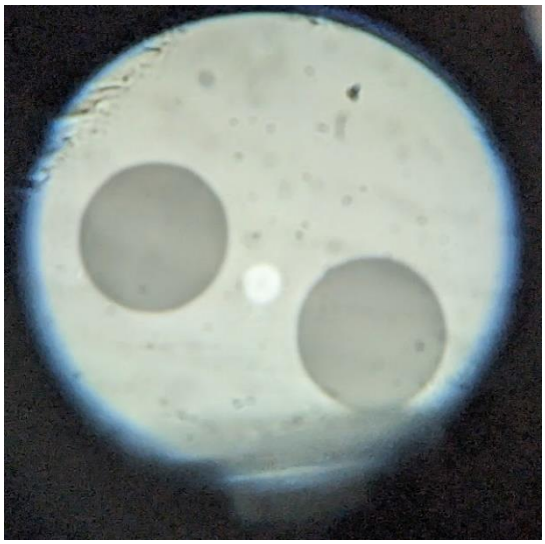


Figure 16: PANDA PM fiber for our Mach Zender Modulator.

The dispersion calculations through the fiber are determined by the wavelength and the length of the optical fiber. One of the components of dispersion length of a single mode fiber is Group Velocity Dispersion, GVD, which is when discrete spectral components of a pulse travel[i] at varying speeds. The pulse can increase in width, which can distort the pulses to blend. To calculate the factors to the dispersion we use the formula:

$$D = -\frac{2\pi c}{\lambda^2}\beta_2$$

With β2 representing the group velocity of a monochromatic wave depending on the wave frequency. The different group velocities of the frequency parts of the wave will cause the pulse to broaden over distance. The spreading of the group velocity is GVD. This equation enables us to see how much the wavelength affects the dispersion of the length of fiber. At the wavelength we are operating at the dispersion length is about 80m, which gives us our limit in how much fiber needs to be in the layout before we start worrying about dispersion.

If this system is characterizing a laser source, strong back-reflections can destroy the laser. To keep that in mind, the fibers in the system were either mounted to the optical board or coiled into a fiber holder organizer. The fibers were also labeled based on the color of the packaging, with the angle polished connector (APC) matching to another APC and a FPC (Flat polished

connector matched to a fiber of the same face. This is to limit back reflections from occurring in the system as well as preventing any optical power from traveling to unwanted areas throughout the system.

**3.2.1.4.4 Sources**

For the case of the demo and initial testing of the FREG, we used a 1550 nm fiber laser which produces solitons as our test source. This was mainly because it was a device which we knew a rough estimate of its pulse duration and repetition rate which could be utilized as a benchmark to see whether our device was working properly overall.

Solitons are single crest waves produced by dispersion and non-linearities in a fiber-based device competing with one another. Solitons are important because they have a flat phase profile. Flat phase refers to the frequency components of the signal not changing with time or propagation. Thus, the FREG will mainly be characterizing optical signals with flat phase profiles.

Lasers are typically comprised of four components: the resonating cavity, the pump source, an amplifying medium, and the output coupler. The pump source will inject an electrical current into the gain medium. The supply of excess electrons promotes the combination of electron-hole pairs (EHPs), where an electron is demoted from the conduction band back to the valence band. During this process, the electron loses energy, and due to the type of semiconductor chosen (direct bandgap), this loss in energy has the possibility of being released as a photon. This recombination process will keep occurring, where electrons with differing energies will produce photons with different energies. We know that photon energy is related to the wavelength of light via:

$$E_{Photon} = \frac{hc}{\lambda} m\lambda = 2L_c$$

(Left) Equation which relates the energy of a photon to its wavelength. (Right) Equation which describes the standing wave condition of a resonant cavity.

The equation on the left is important because until a photon is released with an energy/ wavelength which can resonate within the cavity, optical amplification cannot begin. A produced photon will resonate within the cavity when it satisfies the standing wave condition shown above. In this, we see that the half-wavelength must be an integer multiple of the cavity length for the wavelength of light to resonate in the cavity.

The typical structure for lasers consists of a Fabry-Perot etalon, where the ends of the cavity are comprised of a reflective surface or interface which is engineered to trap the desired photons. Once a photon of this wavelength is produced, it will bounce back and forth in the cavity, and its energy will encourage the production of photons with the same wavelength. This process will continue to multiply until the lasing threshold of the laser is met. The lasing threshold is the minimum gain required for laser operation. The photons are able to escape the cavity via the other mirror of the cavity being partially transmissive.

Laser operation is defined as narrow bandwidth, coherent optical output produced by a resonator. The narrow bandwidth is important because it allows for laser light to experience less dispersion than sources with wider bandwidths, due to the output optical signal not being comprised of as many wavelengths. Fiber lasers, which will be the most common input to the FREG system, consist of a fiber loop which acts as the cavity with an erbium-doped portion which

amplifies energy within it. Fiber lasers are able to achieve mode-locking., which is how we are able to achieve the solid-state production of ultra-short pulses.

Mode-locking a laser refers to the overlapping of many wavelengths of light within a certain range (ex. 20 nm). Each of the overlapped wavelengths of light has a different phase, but these phases overlap such that they are harmonics or multiples of one another, they have fixed relationships. These fixed phase relationships at various wavelengths are what produce ultrashort pulses in the time domain. The wavelengths chosen are not random, they are in fact the longitudinal modes of the laser. Longitudinal modes are all of the modes which can exist in a given cavity length. Additionally, the range of wavelengths is the gain of the amplifying medium. The intersection of the longitudinal modes and amplifying medium's gain spectrum tells us all potential oscillating modes for a given laser.

There is no parts comparison for the sources, as the source is what the system will be characterizing. However, we still found it important to mention characteristics of the source and how it functions as it influences the overall design of the system heavily. There is a table of mode-locked lasers in Section 6.3, as this information was used to determine the specifications of the spectrum analyzer.

### 3.2.2 Optical Spectrum Analyzer

There are many different configurations for optical spectrum analyzers, with trade-offs in complexity, speed, accuracy, supported wavelength range, and sensitivity. The OSA will only measure the average output optical power from the FREG. A concern with OSA measurements for our design is that any nonlinearities or saturation of the sensor can cause inaccuracies in the recorded spectrogram. Thus, we will need to take this into account when designing the OSA.

An optical spectrum analyzer is made up of two main elements: a monochromator and a photodetector. The monochromator can be considered as an optical bandpass filter, as it only allows a certain range of wavelengths to be transmitted or reflected, depending on the grating spacing. The photodetector simply measures the power of the wavelength which has been "selected" by the monochromator. In addition to these elements, there is generally a set of lenses or mirrors for purposes such as collimation and focusing, as well as other optical components to increase the measurement quality. Typical optical spectrum analyzer configurations include the Czerny Turner, Lens-Grating-Lens, Fourier Transform, Littrow, Ebert-Fastie, and Linear Array.

In the Czerny-Turner (CT) configuration, the OSA set-up consists of a pupil, two mirrors, the diffraction grating and the photodetector. The light enters through the pupil/entrance slit, and is collimated by the first mirror, which is typically a curved mirror. This collimated light then travels and hits a blazed grating, which separates the input light into its constituent wavelengths. This light then travels to a focusing mirror, which is again typically a curved mirror, before travelling to the photodetector array, where the optical signal is converted into an electrical signal. The spectrum of the input optical signal can be entirely measured via rotation of the diffraction grating, where rotation in theta can be mapped to the individual associated wavelengths for the sake of spectrogram production.

An LGL or Lens-Grating-Lens spectrometer is very similar to the Czerny-Turner spectrometer, its main difference being that it swaps the collimating and focusing mirrors for collimating and focusing lenses instead.

The Fourier-Transform (FT) configuration has an increased resolution and accuracy at the cost of a more complex set-up compared to the other OSA configurations. It consists of a moving stage with two mirrors facing opposite directions. These mirrors are called retroreflectors. The overall set-up of the FT OSA is interferometric in nature, meaning that it splits the input source, sends each portion of the split beam through a different optical path length, and then recombines it. This process causes the separation of wavelengths since different wavelengths travel at different speeds, thus the extended optical path created by the double-pass through the mirror system allows the wavelengths more time to separate spatially.

The Ebert-Fastie configuration is similar to the Czerny-Turner, where the individual collimating and focusing mirrors are replaced with a single spherical mirror. The Ebert-Fastie's combination of these two mirrors is likely a degradation of the system's performance as it removes a degree of freedom from the optical design. [25]

The Littrow OSA configuration is like the Ebert-Fastie in that it consists of a grating, detector, slit, and a single spherical mirror which both collimates and focuses the beam. However, the order of these components is rearranged. The light sources bounce off the spherical mirror which hits a reflective grating on one side of the light source, and then the reflected light reflects off the mirror and onto a detector on the other side of the light source. This cross-configuration set-up of the OSA may have some performance degradation but is compact.

In a Linear Array configuration, we eliminate the need for a moving grating due to the usage of a line array detector rather than a typical 2-D photodetector. This set-up consists of similar focusing and collimation optics as the previous set-up.; However, it swaps the reflective grating for a transmissive grating and uses a 1-D linear array sensor (also called line array or linear detector array) instead of a plane array sensor. This configuration splits the incoming light through the diffraction grating and focuses that light onto the line array, allowing for the entire desired spectrum to be captured concurrently. The lack of moving parts in the linear array spectrometer also means that this configuration has a faster measurement acquisition time compared to the Czerny-Turner configuration. However, linear array sensors are much more expensive when compared to even the cumulative cost of the Czerny-Turner OSA. Linear array sensors are expensive (~10k) due to their increased responsivity and the fact that they utilize CCD technology over CMOS technology. CCD stands for charge-coupled device and is a slower but more accurate imaging sensor compared to the widely prevalent CMOS devices. This is because CCD devices do not experience the pixel-by-pixel noise that CMOS devices experience due to their per-pixel amplifying transistors. The read-out time on CCD's is slower due to their "fire-bucket brigade" method of transmitting the captured signal, however, this system also ensures uniformity in the read-out. Regardless, for our application, these read-out speed differences (~ms scale) are insignificant as the OSA has no strict speed requirement. Overall, we will build the Czerny-Turner configuration due to its simplicity and low cost.

#### 3.2.2.1 Diffraction Grating (Monochromator)

A diffraction grating can be either transmissive or reflective in nature. An overall understanding of how diffraction gratings work can be extrapolated from the concept of multiple-slit interference.

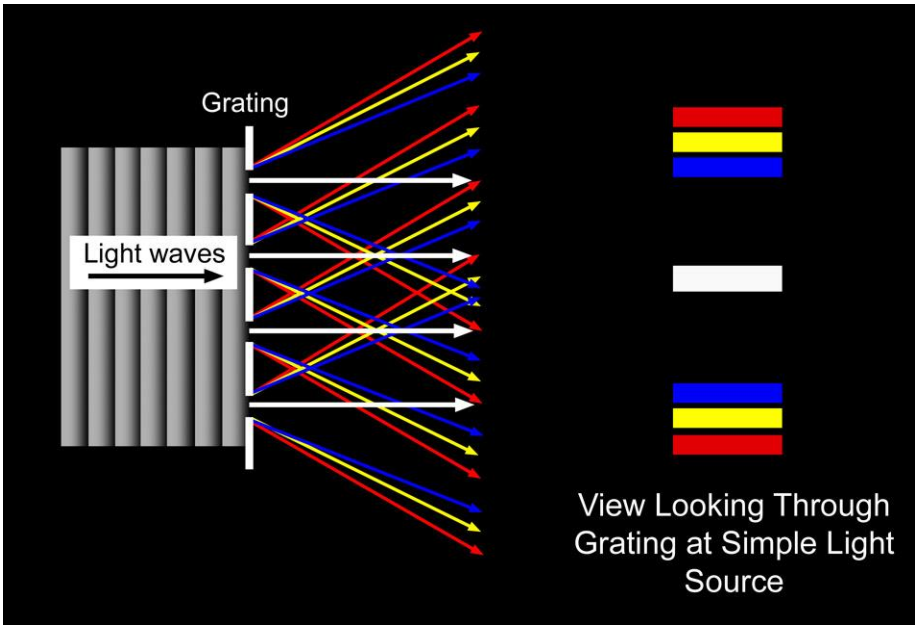



Figure 17: Example of Diffraction Grating Dispersion. Shows the dispersion of light through a diffraction grating, utilizing the conceptual understanding of multiple-slit interference. [69]

Diffraction can be described as the bending of waves around an object, causing spreading of the incident light. Diffraction occurs when the wavelength of the light propagating through an aperture is comparable to the size of the aperture. For example, a typical grating period for a diffraction grating is 100 lines/mm. This equates to 0.1 lines per micron, whereas the wavelength of light propagating through this device would be on the order of 0.4-0.8 microns, which is visible light. Thus, because the wavelength of light is on the order of magnitude as the aperture it is interacting with, diffraction will occur. Generally, the condition for a *diffraction-less* system is the following:

$$D \gg \lambda$$

Where D is the aperture or slit width diameter and lambda is the wavelength of the light incident upon the aperture. The ">>" refers to the aperture needing to be at least two orders of magnitude larger than the wavelength of light interacting with it. Thus, from the example given above, and knowledge of our own system, we see that diffraction will occur using the diffraction grating at our target wavelength.

For this example, we will assume an ideal single-wavelength source. Once the light source passes through an aperture, we can consider the succeeding light as emanating from a a line of point sources that originate along the aperture opening, according to Huygen's principle. This allows us to simplify the understanding of the subsequent interference which takes place in the case that there are multiple apertures along an incident wavefront, each with a specified spacing that does not restrict the interference of the succeeding light, i.e. it is not too large. Because the light is being diffracted, or dispersed, by the narrow apertures, these cones of dispersed light exiting the apertures now only overlap selectively. If one were to place a screen perpendicular to the light propagation, they would see the light intensity has peaks and valleys which correspond to its strength.

The light will be the “brightest” or most intense in regions where constructive interference of the waves takes place, and alternatively will be the least intense where destructive interference occurs. Whether light interferes constructively or destructively depends on the phase of the light interacting. When light waves are in-phase and interact with one another, this produces constructive interference, where the light adds together. Alternatively, when the light waves are 180 degrees out of phase with one another, this is the absolute opposite end of the spectrum where the light destructively interferes, causing a minima in the output power.

Typically, interference follows the diffraction of light off of a device, especially in the case of multiple-slit interference and diffraction gratings. Once the incident light is dispersed, as previously mentioned, the light will recombine depending on how the wavefront of the light interacts. Every wavelength of light is diffracted at different angles. This is due to the inherent size differences of differing wavelengths, meaning they will react differently travelling through the same aperture. This is also a consequence of the previously mentioned Huygen’s principle of the diffracted light being a line of point sources along the aperture opening. If we consider a point perpendicular to the aperture's center, we find that all of the emanating sources are in-phase. This is how the zero-order of diffraction gratings occur. As soon as we move away from this center point however, the light is out-of-phase. In addition to this, because light of different wavelengths will experience sharper or shallower diffraction, this will result in the light being separated in a gradient by wavelength.

The way actual diffraction gratings work utilizes these foundational concepts of interference and diffraction but implements them in altered ways. A transmissive diffraction grating works via changing the optical path length experiences by a plane wave passing through the grating on a periodic basis. Transmissive gratings typically due this via two methods: Reliefs or Volume-Phase Holography.

Surface relief gratings are typically sawtooth shaped variations in the thickness of the surface of the grating. These change the optical path length because the light which travels in a thinner portion of the sawtooth compared to the thicker portions will travel a smaller optical path length. This is due to the refractive index difference between air and the grating material. This difference in optical path length will cause a phase difference of the light, which will influence the subsequent interference of light when it recombines at the output of the diffraction grating. Additionally, because these relief structures are on the scale of the wavelength of the light, this will create the differences in diffracted angles of the light at different wavelengths.

Volume-Phase Holographic (VPH) gratings work via refractive index modulation. They do not have surface grooves, but instead utilize a dichromated gelatin (DCG) film to diffract the light. VPH gratings are typically thicker than relief gratings. Due to their construction, specifically because the DCG film is encased in glass, they are more resilient and efficient than relief gratings, but at a higher cost.

A reflective diffraction grating is composed of alternating strips of reflecting and non-reflecting material on a surface relief structure. This creates the same effect as the slits of a multiple-slit interference set-up. For the chosen Czerny-Turner OSA configuration, a reflective diffraction grating is used, so we will be focusing on analysis of these gratings. For reflective gratings, there exists blazed gratings and holographic surface gratings.

A blazed grating is a special type of ruled grating which concentrates most of the diffracted light into a specific order. It also concentrates the light out of the zero-order, to increase the device efficiency. It accomplishes this control of the light via the component geometry. For blazed gratings, the three important characteristics are the blaze angle, blaze wavelength, and the groove spacing. The groove spacing of the grating determines the output separation of wavelengths from the input optical light. The blaze wavelength is the wavelength at which the grating experiences the maximum efficiency. The blaze angle is the angle between the grating normal and step normal, which enhances the efficiency of the blaze wavelength. It does this by deflecting both the diffracted and reflected portions of the beam in the same direction.

Holographic surface (HS) gratings are similar to typical relief gratings, however, they have a sinusoidal shape rather than a sawtooth shape. However, compared to ruled gratings they are not as efficient for our desired wavelength of 1550 nm. They do overcome some of the problems with ruled gratings, such as ghosting and heavily scattered light, which contribute to unnecessary power losses. However, these HS gratings are more expensive.

The Littrow configuration occurs when the incident and diffracted angles of a grating are equivalent, meaning an n-order beam is retroreflected from the grating. The Littrow configuration optimizes grating efficiency with respect to incident angle. This configuration simplifies the geometry of a diffraction grating, making it possible to easily calculate the grating needed for a particular set-up. Typically, the beam is concentrated into the first order. Additionally, this configuration is utilized in several spectrometer geometries, such as the LGL and Littrow spectrometers.

If utilizing the blazed grating in the Littrow configuration, the following is true:

$$\theta_B = \arcsin\left(\frac{m\lambda}{2d}\right)$$

Where m=1 and refers to the order, and lambda = 1550 nm and refers to the output wavelength. We could graph variation in theta_B with respect to spacing "d" to find the optimal spacing for our desired blazed angle when using the Littrow configuration.

The higher the density of the lines on the grating, the larger the separation of wavelength the input light experiences. For our purposes, 600 lines/mm is sufficient, as this is the typical grating period for gratings which apply to our desired operating wavelength of 1550 nm.

Table 6: Comparison of Reflective Diffraction Gratings

| Model No. | 54-851 | 43-749 | GR25-0616 |
|---|---|---|---|
| Company | Edmund Optics | Edmund Optics | Thorlabs |
| Type | NIR Gold | Ruled Aluminum | NIR Ruled |
| Blaze Angle (deg) | 28.68 | 28.68 | 28.41 |
| Grating Frequency (Grooves/mm) | 600 | 600 | 600 |
| Blaze Wavelength (nm) | 1600 | 1600 | 1600 |
| Efficiency (%) | 80 | 77 | 77 |
| Cost | $112 | $94 | $126 |

For this table, we specifically are looking at the gratings which are 25x25 $mm^2$, however, there are 12.7x12.7 and 30x30 $mm^2$ choices as well. Because these devices have similar grating frequencies and maximum efficiency wavelengths, we will choose the grating with the highest efficiency, since all three devices are around the same price point. Thus, the Edmund Optics 54-851 is the diffraction grating that is selected.

### 3.2.2.2 Photodetector

The photodetector of the OSA does not need to be as fast as the photodetector used in the FREG system. This is because the photodetector in the OSA only needs to measure the output from the FREG, which will be measured as an average value due to the periodic nature and speed of the output. The photodetector of the OSA does not affect the gating functionality of the input in any form. Therefore, we cater the OSA photodetector only to the optical wavelength range and desired wavelength of the input, as well as the typical input power. The input wavelength range for the FREG will likely be quite narrowband as though mode-locked lasers are made up of many frequencies, these frequencies are typically within a spectral width of ±10-30 nm. The operating frequency and range of the detector allows us to pin down the best photodetector material. The typical input power is important to take into account, because if the input power is especially low, we run the risk of the signal being obscured by noise.

A possible candidate for the OSA photodetector would be an InGaAs photodiode with thermoelectric cooling. Thermo-electric cooling is necessary to reduce thermal noise, which assists in the accurate measurement of the signal. We have conducted the part search for this item after calculating the average value of the output from the FREG and the needed diffraction grating for the OSA. The average output from the FREG is necessary for a noise analysis on the photodetector, whereas the diffraction grating design will be needed so we know the size of the separation between the orders which the grating will diffract the light into, and subsequent spectral resolution. We want our sensor to be able to capture the 1st order diffracted light, thus it must be wide enough to do so.

Table 7: Photodiodes for the OSA

| Model No. | PDA20CS2 | PDA20C2 | PDA10DT(-EC) | PDA10CS2 |
|---|---|---|---|---|
| Company | Thorlabs | Thorlabs | Thorlabs | Thorlabs |
| Bandwidth Range | DC-11 MHz | DC-5 MHz | 500 Hz-1 MHz | DC - 13 MHz |
| Gain (50Ω) | 0.75 kV/A - 2.38 MV/A | 175 kV/A | 1.51 kV/A - 4750 kV/A | 0.75 kV/A - 2.38 MV/A |
| NEP | 1.95 - 61 $pW/Hz^{1/2}$ | 22 $pW/Hz^{1/2}$ | 2.11 $pW/Hz^{1/2}$ @ DC - 2.5 kHz | 1.91 - 46 $pW/Hz^{1/2}$ |
| Active Area ($mm^2$) | 3.14 (Ø2.0 mm) | 3.14 (Ø2.0 mm) | 0.8 (Ø1.0 mm) | 3.14 (Ø2.0 mm) |
| Wavelength Range (nm) | 800-1700 | 800-1700 | 900-2570 | 800-1700 |

| | | | | |
|---|---|---|---|---|
| Cost | $631.97 | $691.37 | $2,381.77 | $476.36 |

We see a comparison between several lines of Thorlabs photodiodes. These are from the free-space, biased, and free-space OEM packaged lines respectively. We see that the 20CS2 and PC4 models have a switchable gain, which would add flexibility to our design if utilized properly. We see that the fain chosen affects the NEP of the detector, which is a parameter we would like to keep low. Overall, we find that unless the OEM packaged PDA10CS2 will be particularly difficult to work with or connectorized, we will likely go with it due to its low cost yet versatile specifications. We also highly prioritize the size of the active area when deciding on the correct detector, as we will be using this detector in the spectrum analyzer.

#### 3.2.2.3 Motors

The motor in the OSA will need to be quick, but the biggest factor that is desired is how precise the motor can be. The motor for a Czerny Turner Monochromator has to rotate in order to change the angle of the diffraction grating. The diffraction grating will rotate to separate the different wavelengths in various directions. This will enable us to see the center wavelength when we rotate the stage the diffraction grating sits on. There are various types of motors that are potential to this project.

Thorlabs has a stepper motorized rotary mount known as the K10CR1 [26]. This specific rotary motor has a maximum speed of 10º per second, which is reasonable within our desired speed. The speed of the motor doesn't have to be incredibly fast compared as the rest of the setup, rather we are looking for precision of the motor. The motor can go 360º with the increments being 0.03º per line. This enables us to have some control in how small we want to have the steps in order to get to the center wavelength of the laser. The step size according to Thorlabs has the confidence level of 99.5% with less than a 10% error. This motor is powered through a program through a USB, which we can control the movements of the motor on a computer. The device itself is the max length of 4.2 inches, which enables us to have the setup maintain a small and concise layout. Overall, the price of the motor is flaw we see as it is priced to be over $1,500 on the website, which makes it above the desired budget. The rest of the specifications however, do reach our desired constraints.

The other motor from Newport called the CONEX-AG-PR100P [27], is a piezo motor that has a rotary stage along with a controller and driver. The speed on this piezo motor is about 1.5º per second and an increment size of 1mdeg. The travel range for this rotary motor reaches to 340º with a USB as the computer interface. This piezo rotary motor runs with direct coder feedback along with a closed-loop piezo motor controller. This motor is not only used for positioning targeted polarized optics, but it can also be used as a rotation stage for precision positioning. The rotary stage has its own built-in direct read encoder which enables us to repeat the turns at high angular positions with precise movements. The device is also very compact, this is beneficial for the set up because this can make the OSA layout more concise.

The final motor that is to be determined for the OSA was the StepperOnline stepper motor. This rotation stage does not have its own controller or driver, instead the PCB will power the motor as well as change the rotating angle the diffraction grating will go based on the input of the time delay line. The main focus the motor has to do is perform extremely precise movements in order to get an accurate reading of each sweep. The range is larger than the piezo driven motor as well

by 60º with the stepper motor, it can continuously rotate 360º while the piezo can only do 340º. This gives us more room to do smaller increment measurements with higher accuracy.

When comparing all of these motors, the piezo drive motor is slightly slower than the Thorlabs stepper motor, however there is a higher sensitivity to the piezo drive motor because of its ability to have a direct read encoder in the stage. There is a higher repeatable angular motion in the rotary motor as well. While speed is a strong specification, the higher sensitivity to the wavelength is what we desire for the set up in order to maintain better accuracy in capturing the pulses.

Table 8: Comparison of Rotary Motors

| Model | AG-PR100P | 14HR05-0504S | PRM1Z8 |
|---|---|---|---|
| Company | Newport | Amazon | Thorlabs |
| Max Rotation Velocity | 1.5º / second | 3º / second | 25º / second |
| Repeatable Incremental Motion | 0.02º | 0.9º | 0.03º |
| Range | 340º | 360º Continuous | 360º continuous |
| Home Location Accuracy | +/- 0.2º | N/A | +/- 0.2º |
| Cost ($) | $2,492 | $23 | $1,037.67 |
| Lead Time | No lead | No lead | 7-10 Days |

## 3.2.3 PCB

**Design Integration**

The PCB functions as the central processing unit between the time delay line, PC and grating motor in the FREG system. A communication link must first be established through a Universal Serial Bus (USB 3.0) connection that sends data to a microcontroller at a low frequency signal and back to the time delay line. The Texas Instruments MSP430 series are not configured to run USB 3.0 only USB 2.0 which will alter the designing of the connection between the delay line. The baud rate for the delay line is 9600 which is a constant, so in theory a microcontroller with 12-bit SAR ADC type is sufficient to handle the transmission of data to and from the delay line. Fortunately, a USB controller USB interface hub is configured to support USB 3.0 and 2.0 operations which is vital for the delay line and computer connections. Incorporating this hub may result in technical difficulties during the designing phase since it an additional component that would need to be configured with a MCU to allow USB 3.0 connections. The problem with using a hub to obtain the USB 3.0 connection was the excessive PCB design required to implement the component on the board. This would result in a third layer being added to facilitate all the necessary components and wiring procedures. The alternative method was to simply develop multiple USB to UART connections using a bridge interface for both PC and time delay line ports. This technique allows the utilization of USB 2.0 granted the MCU component is compatible and since the baud rate specification for a 2.0 connect is about the time delay baud rate constant the design can be implemented on the top layer the board with leaving sufficient room for the wiring.

USB 3.0 is a high-speed transmission that requires specific routing topology techniques to ensure impedance control. Additionally, the critical path between the microcontroller (MCU) and

the USB connector is important and orientating the MCU interface connector to be adjacent to the USB port which will represent the coupled Differential pair (D+, D-) signal traces carrying the data to and from the delay line and a power and ground connections. Furthermore, positioning the MCU close to the USB port is best for reducing trace length distance. A FR4 material based typically has a dielectric value of 4.8 core which results in a propagation delay of 150 ps/inch. Based on the rise time provided in the 'USB 3.0 standard by Tektronix MOI for cable tests' indicates a rise time of 50psec while placing a 25% critical length limit to the routing of the traces. The odd impedance (Zo) along the traces will be the major concern when positioning each component on the layout for the PCB. Defined cable impedance is also a factor to consider that will affect the odd or differential impedance of the PCB. The USB 3.0 typically transmits data at 5Gbit/s which will result in using a thickness of the trace width between 1 - 0.8 millimeters for proper high speed routing standard procedure. The ideal technique for avoiding complications would be to route the traces together to achieve the required natural coupling of capacitance and inductance to hit the odd impedance and differential impedance benchmark. The electric field coupling between the D+ and D- will determine the impedance benchmark and adding ground traces around the differential pair traces lowers the trace width required which makes the design process more manageable. The differential impedance target is 90 Ohms with an ideal 10 mil width trace and enforce clearance and trace gap of 5 mil which ensures that manufacturers can fabricate the PCB reliably. Pull-up or pull-down resistors will also be factored in based what is specified in the data sheet when selecting the actual USB port component that will be used in the prototype. A two-stage voltage regulator system will be implemented consisting of a buck-switching regulator that will convert 6-15V to 5.5V or 3V. Additional low dropout regulators may be incorporated depending on the overall power supply demands of each component.

The grating motor configuration consists of a 4-channel terminal A and B are the positive and negative connections for the 6V DC motor and a Vin and ground terminal for external power source if needed. The microcontroller will need to have a PWM connectivity to avoid any connection or power distribution issues. The grating motor comes with an Agilis-P Controller with Encoder Feedback removing the issue of designing a motor controller to execute specific instructions transmitted by the MCU. The positioning of the power supply connector will be on the opposite end of the PCB to avoid excessive heat or noise from affecting the high-speed components. The wires from motors will be attached to the PCB manually by a power supply block that has a screwable wire lock mechanism to hold the two wires into place. The voltage regulator for the power supply will determine the amount of thermal management required on the PCB. A boost step-up regulator will be connected to the DC motor power supply to ensure that the grating motor is constantly being supplied 6V requirement throughout the system's operation. Linear regulator will be avoided in this specific power supply design because of the inefficiency and high heat loss which can result in larger ripples creating more noise on the PCB with fast-speed components. Reduction in noisy digital circuits increases the efficiency of the power distribution network.

The third connection between the PC and PCB via USB interface connection that uploads instructions to the MCU by sending code from the PC using MATLAB software. The completion of the executed operations results in a data matrix of information displayed on the PC signifying that the system is operational and functioning as intended. The connection to the PC will be made using a USB type B connector from the PCB to a USB 2.0 port on the computer. Like the delay line USB port, various design techniques will be implemented to ensure a balance impedance on

the board in addition to noise reduction and heat dissipation. Ideally, the type B connector and USB connector will be positioned relatively close to each other per design constraints procedures of keeping all high-speed components in one area. The MCU will be positioned close to both the ports to reduce trace length connectivity ensuring typical PCB procedures regarding fast interfaces are maintained on the PCB.

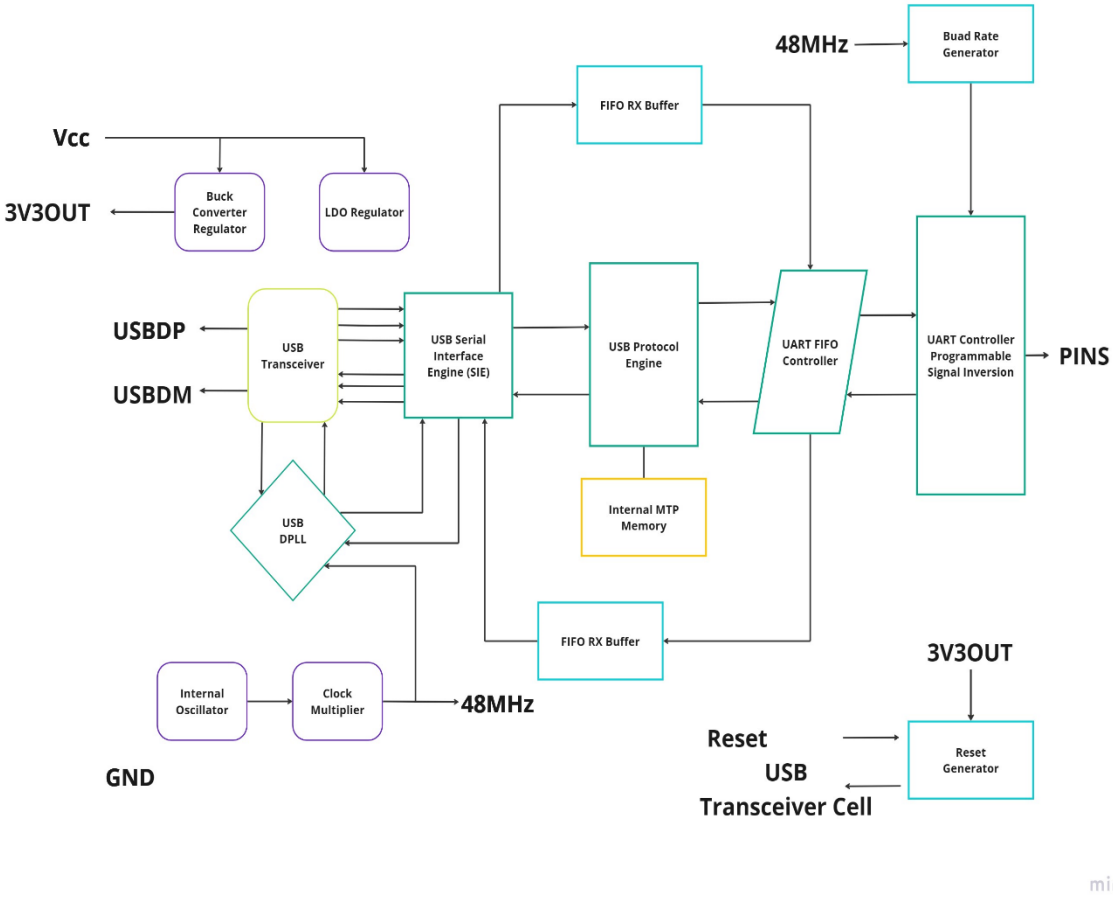



Figure 18: USB-to-UART Bridge Interface.

### 3.2.3.1 JLCPCB Manufacturing and Assembly Capabilities

The manufacturing specifications for JLCPCB restrict my design parameters which identifies my criteria and constraint for what would be acceptable in the schematic layout of my PCB. The PCB layout will feature two-single sided layers, ideally the top layer consisting of all electrical components and the bottom layer would be the ground and various connections. On the site ‘PCB Manufacturing & Assembly Capabilities’ [29] are the following parameters regarding PCB assembly. The thickness of the layers can range from 0.8mm-1.6mm with a single size PCB measuring 10x10mm-510x460mm and panel size of 70x70mm-250x250mm. This opted design plan allows for more flexible and available spacing between all the traces which is a huge factor

during the fabrication process. The PCB material base is made from a flame-retardant (FR-4) epoxy resin and glass fabric composite. The minimum impedance control includes a tracing width/spacing of 3.5mil, a minimum via of 0.2mm, a ball grid array of at least 0.5mm and an IC Pin spacing of 0.4mm. The reflow temperature is fixed at 255+/- degrees Celsius. The controlled impedance stackup usually accounts for three different variables: the Prepreg dielectric constant, solder mask parameters and core dielectric constant. JLCPCB permits four different prepreg dielectric constants, however the core dielectric constant is set to 4.6 and the coating about the substrate and trace are fixed to specific values provided in the multilayer high precision impedance control table. The assembly lead time is approximately one to three days depending on whether JLCPCB constructs the panel using V-cut. The reason for selecting JLCPCB as the manufacturer is their extensive library of assembly parts and fast PCB printing lead times. If there is an issue regarding a specific component in the PCB, modifying and sending out to be refabricated is quick and easy. Additionally, JLCPCB allows pre-orders providing security in obtaining parts needed in advance, reducing lead time on fabrication.

### 3.2.3.2 RF Development

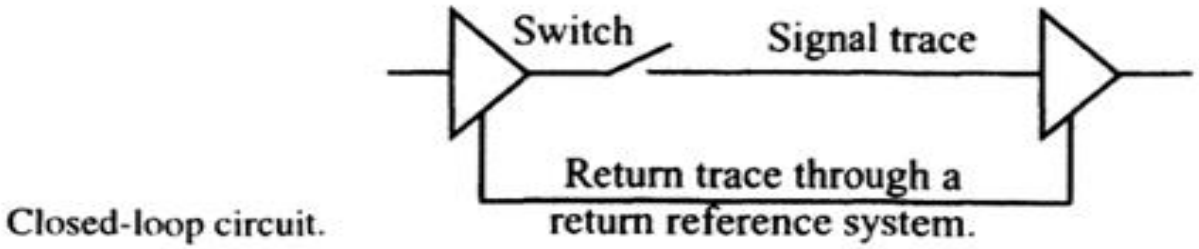



Figure 19: Closed-loop Circuit

An important and crucial aspect when designing the PCB is estimating signal propagation delays from the source to the output by modifying the trace impedance and length to ensure a controlled electrical flow on the panel. Radio frequency plays a key factor in calculating the capacitance between the traces, free space, and the ground plane affects the transmission of signals to its destination. In the book 'Printed Circuit Board Basics' [30] states "whether it is between the leads of a component, between a component and metal structure (chassis), a PCB and a metal enclosure, or any electrical item, relative to another electrical item, parasitic capacitance will be present. We frequently forget that air is a dielectric. Propagation of RF waves usually occurs through free space, or air." [30]. To eliminate RF energy in the PCB design, flux minimization through combination of a clockwise and counterclockwise field implementation can result in a cancellation effect. Utilizing stack up assignment and impedance control when dealing with multi-layers allows for a RF ground path to exist, Reducing RF currents within traces through reduction of RF drive voltage from clock and capturing magnetic flux into the OV-reference system to reduce component radiation. Traces have a finite impedance value, furthermore, utilizing Ohm's Law in time and frequency domain with a basic understanding of how Electromagnetic Interference works is feasible for eliminating potential disruption in the circuit. The following laws and equations must be considered when dealing with PCB Electromagnetic capabilities along with a figure

displaying the principles of Kirchhoff's and Ampere's laws, a closed-loop circuit must be present if the circuit is to work. Kirchhoff's voltage law states that the sum of the voltage in a closed path must be zero in the circuit:

Ohm's Law (time domain) $V = I \cdot R$

Ohm's Law (frequency domain) $V = I \cdot Z$

Impedance Z = $R + jX_L + \frac{1}{jX_c} = R + j\omega L + \frac{1}{j\omega C}$

where: $X_L = 2\pi fL \quad X_L = \frac{1}{2\pi fC} \quad \omega = 2\pi f$

$$|Z| = \sqrt{R^2 + jX^2} = \sqrt{R^2 + j(X_L - X_C)^2}$$

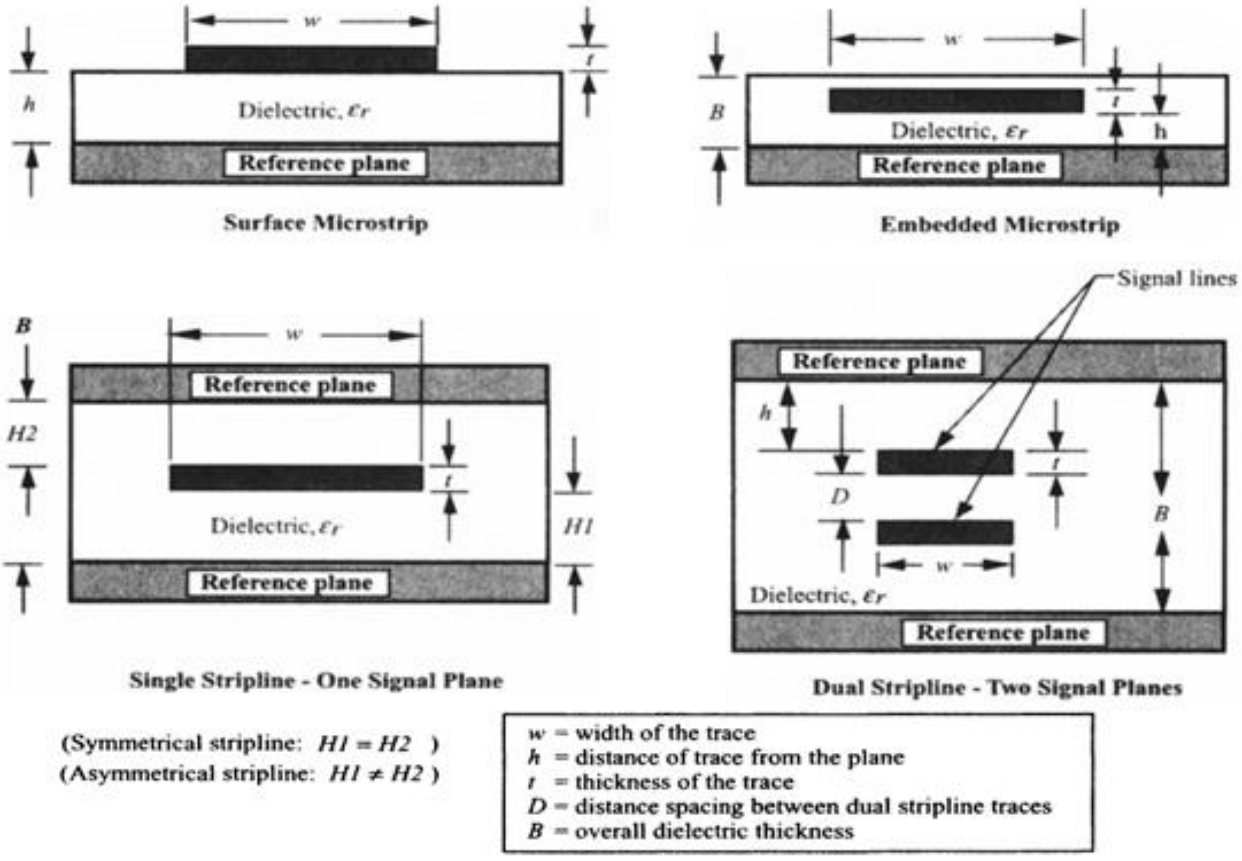



Figure 20: PCB Routing Topology

Routing topology configuration designing for PCB are separated into two factors: Microstrip and Stripline. The microstrip is essentially the trace on the top and bottom of the layers of a PCB that aids in the suppression of RF energy being produced. Additionally, less capacitive coupling and lower propagation delay between the source and load resulting in faster signals. Subsequently, Stripline is the placement of signal layers within two solid planes providing noise immunity from RF emissions. The signal traces cause distributed resistance, capacitance, and inductance after reaching a frequency above 500MHz. In the book 'Printed Circuit Board Basics' indicates that "At higher frequencies, the dimensions of the transmission line play an important

role in defining performance. Changing any dimension can dramatically alter board performance." [30] The following images exhibits routing topology configurations that are present. Suppressing RF is energy is more optimal than containing it through the usage of voltage and ground planes embedded in the PCB design since it has a direct correlation to reducing high frequency power distribution. Determining the required layers for functionality is vital to identifying impedance control, component density, routing of buses, number of (nets) traces to be routed, signal separation and noise immunity. Radial migration which occurs through the transfer of energy in a circuit from a high-bandwidth to low-bandwidth area can result in an intrinsic propagation delay. Fortunately, the circuits usually cascade from the CPU area to I/O allowing filtering of the high-bandwidth spectral components from the system and I/O circuits.

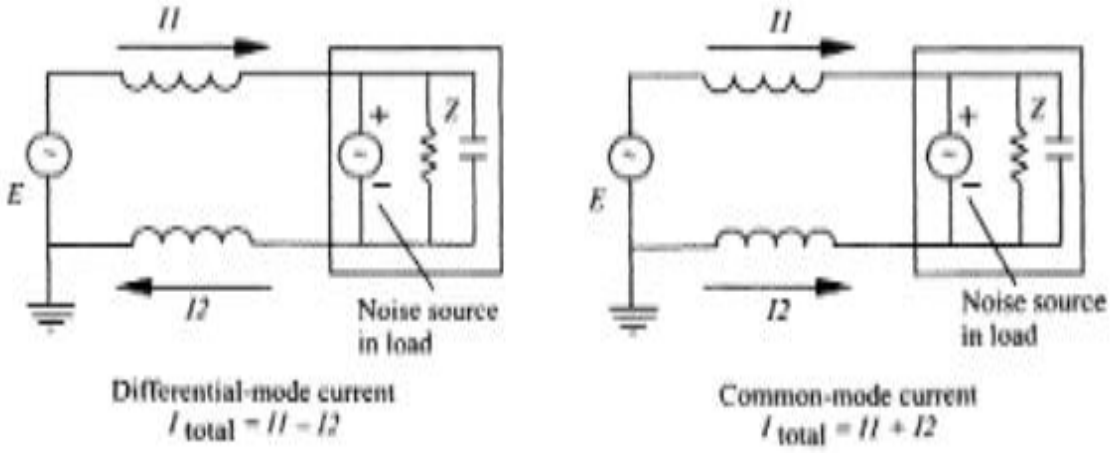



Figure 21: Common- and differential-mode current

### 3.2.3.3 Common Mode and Differential Mode Current

Another contributor toward RF energy is differential and common mode current that flows through the traces in the PCB. The traces in the schematic are all source to load route indicating differential mode current since its main function is to carries data throughout the circuit. The PCB schematic layout should be designed with RF return paths close to the trace routes to oppose and cancel out all minimal interference induced by the signal transmissions. The common-mode current is present on the traces responsible for the signal and returning path and calculating the sum of current identifies the total amount of RF energy in the PCB. To prevent common-mode current, incorporating a differential-mode cancellation system is necessary by making sure the differential signals are leading in the opposite direction. The density distribution of RF current depends heavily on the common impedance that is shared between the trace and plane causing mutual coupling. In chapter 2 of 'Printed Circuit Board Basics' [30] it states "When the distance spacing is far apart between trace and plane, the loop area between the forward and return path increases. This return path increase raises the inductance of the circuit where inductance is proportional to loop area" which will help to control the PCB current when adjusting the traces and return path routes for optimal functionality. The formula below is used to calculate density distribution:

$$I(d) = \frac{I_o}{\pi H} \cdot \frac{1}{1 + \left(\frac{D}{H}\right)^2}$$

Where $I(d)$ = signal current density (A/in or A/cm) $I_o$ = total current (A) $I(d) = \frac{1}{1+\left(\frac{D}{H}\right)^2}$

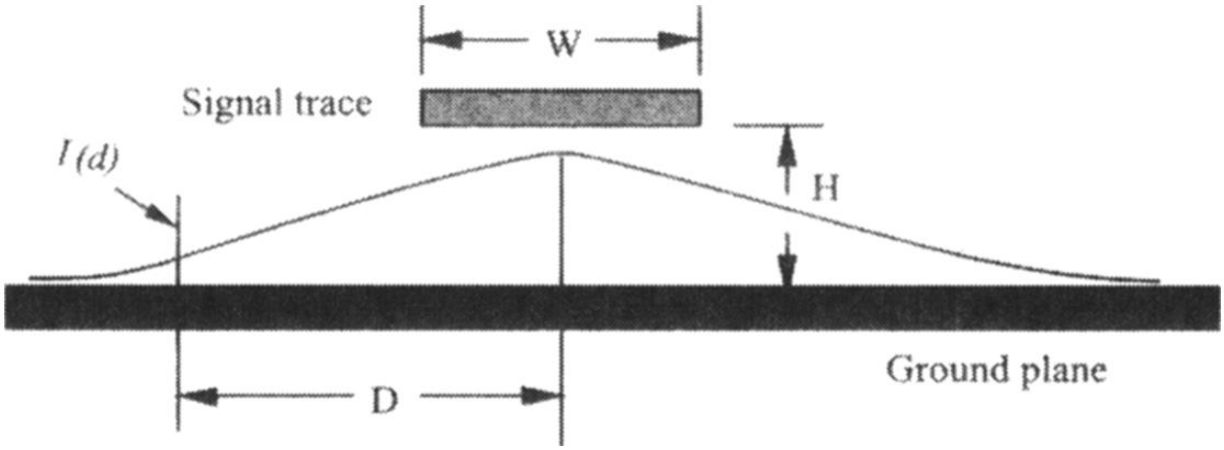
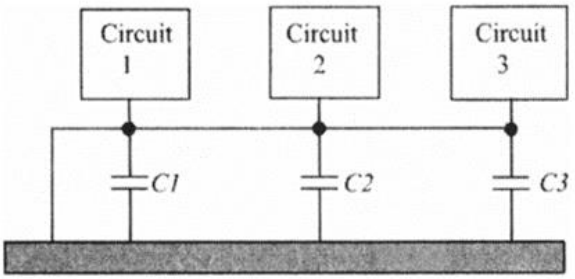
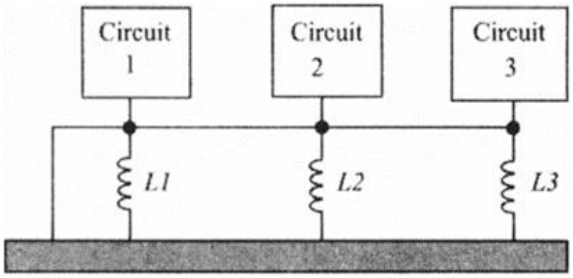



Figure 22: PCB current control

Grounding methodologies are an important factor for the circuit design layout and can affect trace width and spacing. Single-point grounding techniques would not be a viable option when routing my traces to a reference voltage since it is commonly used in low frequency circuits consisting of one megahertz or less. Furthermore, single-point grounding leads to high impedance which is bad for PCB designing and results in RF increase which is the opposite of our expectation. Utilizing both multipoint and hybrid grounding configurations would be the most feasible option when designing the schematic since the second layer of the PCB is a00 reference plane. Depending on each component, multipoint and hybrid grounding will be implemented to reduce signal noise, RF energy and impedance of the board. Keeping the ground leads short plays a vital role in minimizing lead inductance which can only be achieved by incorporating a multipoint or hybrid grounding system. Thus, negating voltage potential interconnect wires and preventing common-mode current generation. Each trace can add inductance to a circuit based on the thickness and width of the trace; accounting for these factors can significantly improve signal quality and RF suppression on the board by coupling the current of the signal traces to the reference voltage.




Hybrid grounding—capacitive coupling




Hybrid grounding—inductive coupling

Figure 23: Hybrid grounding methodologies

Subsequently, the ground and signal loops can be a major contributor to negating RF energy. Relocating high speed components should be positioned close to the ground to divert unwanted RF energy to the reference voltage. Incorporating all these measures avoids the use of containment implementation which often results in a more complex PCB layout design and electromagnetic interference. The aspect ratio between the ground connections can cause unwanted coupling of peripherals and components if the ground stitch connection is insufficient. Creating subsections for component placement will minimize signal trace lengths and creation of antennas while strengthening the integrity of the signal transmissions. All subsections should have a ground connection to chassis to ensure that short trace routes using functional partitioning.

### 3.2.3.4 Bypass and Decoupling

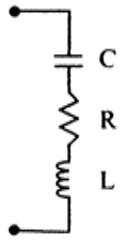
The quality of power distribution is key in the design process to ensure that all components minimum requirements are met throughout the PCB. Three major consisting of the power and ground planes, components and internal power connections determines the final efficiency and heat dissipation during clock and data transition while executing an operation. Accounting for proper decoupling implementation ensures low impedance is present which is a major constraint when designing. Including capacitors into the PCB will allow me to negate this constraint through various bulk, bypass, and decoupling applications. Calculating all capacitors value and selecting a proper dielectric material of the capacitor determines the efficiency of the PCB. Placing the capacitor by the IC's pin to minimize the distance between traces and component while supplying adequate power to IC's when there is a voltage drop are the first approach with each circuit, however the PCB has two layers which allows for more flexible methods in separating all AC and DC signals. Implementing bypass regulators can help infiltering unwanted energy and noise in the circuit. The bulk application will be utilized to maintain DC voltage and current when capacitive load is high. Series and parallel resonance circuits will be applied depending on the power transfer factor from the supply to components, impedance at designated signals and current level through transmission along traces to components.

$$X_L = X_C$$

$$\omega L = \frac{1}{\omega C}$$

$$\omega = \frac{1}{\sqrt{LC}}$$

Series resonant circuit.




$$\omega L = \frac{1}{\omega C}$$

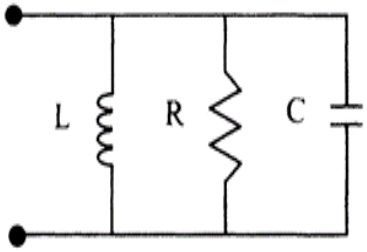



Figure 24: Series resonant circuit

Impedance of series RLC:

Impedance value of a capacitor: $|Z| = \sqrt{(R_s)^2 + \left(2\pi fL - \frac{1}{2\pi fC}\right)}$ $f_0 = \frac{1}{2\pi\sqrt{LC}}$

Where: $Z = impedance\ (\Omega)$

$$R = equivalent\ series\ resis\tan c\ e - ESR\ (\Omega)$$

$$f = Frequency\ (Hz)$$

$$L = equivalent\ series\ induc\tan c\ e - ESL\ (H)$$

$$C = Capaci\tan c\ e\ (F)$$

Furthermore, selecting the appropriate type of capacitors are essential to using the bypassing and decoupling technique. The storage capacity and discharge frequency must be calculated based on the clock speed of the circuit. Current requirements for each component should be identified first before implementing any decoupling and bypass application. The goal in assessing the current requirements is to look at steady-state current requirement during operation, the capacitive load transmission through the traces to components, cycling switches that occurs during recharge state, and the output change switching current that remains. The book on 'Bypass and Decoupling' cites "A capacitor remains capacitive up to its self-resonant frequency. Above self-resonance, the capacitor starts to appear as an inductor due to lead length and trace inductance. Inductance minimizes the ability of the capacitor to decouple or remove RF energy that exists between power and ground." [30]. The table demonstrates typical values for capacitors based on the frequency present in the circuit. The types of capacitors are electrolytic, tantalum, and ceramic each having their own distinct characteristics and capabilities:

Energy storage equation

$C = \frac{\Delta I}{\Delta V/\Delta t}$ where: $\Delta I = current\ transient$

$$\Delta V = voltage\ change(ripple)$$

$$\Delta t = switching\ time$$

The ceramic capacitor is a multilayer dielectric device with a fixed-low value. The capacitor has a low equivalent series resistance, compact package size and is quite affordable. While this type of capacitor is commonly used in numerous electronic applications it is not a suitable option for PCB designing due fragility of the dielectric material used to make capacitor and generate unwanted acoustic emissions. In 'Acoustic Phenomena in Damaged Ceramic Capacitors' [31] indicates "Acoustic emission generation in MLCCs is a well-known phenomenon. It is caused by piezoelectric behavior of barium titanate (BaTiO3), which is a typical dielectric material in type II MLCCs. When subjected to ac voltage, an MLCC starts to vibrate, and the vibration amplitude is greater near the resonance frequencies of the MLCC body.", which changes certain properties leading to faults in the capacitor. Utilizing a ceramic capacitor could result in detrimental malfunction of various components when executing operations due to ineffective bypass or decoupling application.

Next, tantalum capacitors have great stability at high temperatures with a high capacitance, large equivalent series inductance and low equivalent series resistance. Unfortunately, tantalum capacitors are prone to failure due to fast switch on from a low impedance circuit or a current surge during operation. The paper 'Derating of Surge Currents for Tantalum Capacitors' [32] explains that "Tantalum capacitors are typically used for reducing noise and stabilizing DC voltage in the power supply lines. When the power is turned on, high inrush currents through the capacitor can cause so-called surge current failures. For solid tantalum capacitors with manganese oxide cathodes these failures result not only in a short circuit in the system but can also cause ignition due to the exothermic reaction of tantalum with oxygen generated by the overheated MnO2

cathode layer." [32]. The failure of the capacitor can result in a short circuit in the PCB leading to increases in heat resulting in a fire if failsafe are not implemented correctly.

Subsequently, aluminum electrolytic capacitors are the best options when design PCB based on the large capacitance value, low equivalent series inductance and equivalent series resistance which make it suitable for bypassing low frequency signals and storing large amount of energy. The article on 'Electrolytic capacitor: Properties and operation' [33] states "They have higher volume efficiency due to a significantly lower minimum dielectric thickness than all the other capacitors. However, they have a high internal resistance as well as an inductance limiting high frequency performance and low temperature stability." [33]. This type of capacitor is a good selection for power supply noise filtering and handing self-resonance frequency. Low impedance allows for more current flow to components during drastic change in voltage. The voltage and ground level remains at a stable reference value preventing surges from disrupting the power distribution within the PCB. The decision to separate the power and ground plane network helped in reducing potential errors such as spacing issues or RF development mentioned earlier. Additionally, aids with keeping a balance within the power distribution network so which also plays a factor in common-mode energy. The equation referenced below demonstrates how to calculate capacitance of the ground and power plane in the PCB. Proper selection of layer stack up can negate the use of high frequency and low frequency decoupling through adequate placement of ground and power plane in a reasonable proximity. Moreover, component placement of I/O and their interconnections directly impacts RF emission. All I/O will be separated from high bandwidth RF components to prevent any interference during transmission.

Power and ground plane capacitance

$$C = \frac{\epsilon_o \epsilon_r A}{d} = \frac{\epsilon A}{d}$$

Where C= capacitance between power and ground planes (pF)

$\epsilon_o$ = permittivity free space $1/36\pi \cdot 10^{-9}\ F/m = 8.85pF/m$

$\epsilon_r$ =Relative permittivity $\approx 4.5$

$A =$ Area of parallel plates$(m)^2$

$d =$ Distance between plates$(m)$

Electrostatic Discharge protection (ESD) present in I/O connections is another area where certain applications will be incorporated to prevent any disturbances within the system that can lead to failure or excessive heat development. The three key points of interest that will be addressed are discharge into the circuit, direct discharge into the ground system, and indirect discharge. All these discharge events can be countered by reducing the filed coupling techniques. Filtering the source and load, reducing the coupling by separating components from each other, orientating devices perpendicular to areas known to have electrostatic discharge are essential to ensure a safe and functional PCB. Additional techniques are available for multilayer PCB which influenced the design choice such as: keeping low impedance connection by including sufficient ground pins, reducing the distance of power and ground traces and placement of power and ground planes should be adjacent to each other, fill both layers with copper at ground potential, and implement transient protection devices to chassis ground. Chapter six on Electrostatic discharge protection in

'Printed Circuit Board Basics' cites that "Use of multilayer PCBs provides J0 to 100 times improvement over two-layer boards for protection against electromagnetic fields from an indirect ESD event. Locate the first ground plane as close to the signal routing plane as possible. This placement allows ESD to be coupled to a lower impedance reference, thus minimizing ESD energy from reaching signal traces." [30]. Because ESD is difficult to filter out once it is entering the board and the only way to resolve the problem would be to introduce an additional filtering method. This then leads to a spacing problem of trying to fit all the power and grounding network on one PCB.

### 3.2.3.5 Microcontroller Selection

| Table 9: Interface controller connection | | | |
|---|---|---|---|
| Model | PTN5150AHXMP | TUSB8020BPHPR | FUSB30BTMX |
| Company | NXP USA Inc. | Texas Instruments | Onsemi |
| Protocol | USB | USB | USB |
| Function | CC logic for USB Type-C controller | Two-port USB 3.0 controller | Type-C Controller |
| Voltage Supply (V) | 2.7 ~ 5.5 | 1.1, 3.3 | 2.85 ~ 5.5 |
| USB | Type C | 3.0 | 2.0/3.1 |
| Operating Temperature (°C) | -40 ~ 85 | 0 ~ 70 | -40 ~ 85 |
| Cost ($) | 1.15 | 6.55 | 0.77 |
| Lead time | 15 weeks | 6 weeks | 32 Weeks |

The main concern that surfaced regarding interface connection was how to develop a PCB with multiple USB to UART connections. Most MCU are not compatible with USB 3.0 connectors and would require additional design technology such as an USB controller USB interface hub capable of merging the connections to achieve a successful USB 3.0 link. The TUSB8020BHPR controller was the only suitable option for the delay to MCU interface since the delay line had a constraint of being a USB-to-USB connection. The MCU to PC connection was more flexible in the sense that any of the controllers was compatible with the design and the more viable options would be come down to the complexity of integration requirements along with accessibility to the component.

| Table 10: USB-To-UART Interface | | | |
|---|---|---|---|
| Model | FT231XS-R | CP2104-F03-GM | FT234XD-R |
| Company | FTDI, Future Technology Devices International Ltd | Silicon Labs | FTDI, Future Technology Devices International Ltd |
| Function | IC USB Serial Full UART 20SSOP | IC SGL USB-To-UART Bridge 24QFN | IC USB Serial Basic UART 12DFN |
| Protocol | USB | USB | USB |
| Function | Bridge, USB to UART | Bridge, USB to UART | Bridge, USB to UART |

| | | | |
|---|---|---|---|
| Interface | UART | UART | UART |
| Standard | USB 2.0 | USB 2.0 | USB 2.0 |
| Voltage supply | 3.3 ~ 5 | 1.8, 3 ~ 3.6 | 2.97 ~ 5.5 |
| Current supply | 8mA | 17mA | 8mA |
| Operating Temperature (°C) | -40 ~ 85 | -40 ~ 85 | -40 ~ 85 |
| Cost ($) | 2.34 | 5.43 | 2.26 |
| Lead time | 12 weeks | weeks | 12 weeks |

The USB-to-UART bridge is an important interface requirement of the system to for it to function. The following components meet the specifications for the time delay line and the PC connections. The Future Technology Devices International Ltd options had the same application regarding its capabilities. The major differences between the FT231XS-R and the FT234XD-1 were the voltage supply and cost of the components. The Silicon Labs interface was also a great selection but was not chosen due to a recommendation regarding the FTDI models having a wider range of specifications that was more aligned with the PCB design. The FT231XS-r ultimately was the component selected because it had more applications compared to its counterparts and satisfied the design parameters of the interface connection.

| Table 11: Microcontrollers | | | |
|---|---|---|---|
| Model | MSP430FR6989 | MSP430F6659 | STE32F401CCU6TR |
| Company | Texas Instrument | Texas Instrument | STMicroelectronics |
| Core Processor | MSP430 CPUXV2 | MSP430 CPUXV2 | Arm® 32-bit Cortex®-M4 |
| Core Size | 16-bit | 16-bit | 32-bit Single-Core |
| Frequency (MHz) | 16 | 20 | 84 |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT | Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT | Brown-out Detect/Reset, DMA, I2S, POR, PWM, WDT |
| Memory (Kbyte) | 128 | 512 | 256 |
| Program Memory Type | FLASH | FLASH | FLASH |
| RAM Size | 2 | 66Kx8 | 64Kx8 |
| Data Converter | A/D 16x12b | A/D 16x12b; D/A 2x12b | A/D 10x12b |
| Voltage supply (V) | 1.8 ~ 3.6 | 1.8 ~ 3.6 | 1.7 ~ 3.6 |
| ADC type | 12-bit SAR | 12-bit SAR | 32-bit Cortex |
| Number of ADC channel | 16 | 12 | 11 |
| Number of GPIOs | 83 | 74 | 81 |
| Features | Advance sensing, DMA, LCD, Real- | DAC, LCD, Real-time click | CPU with FPU, Adaptive real-time |

| | | | |
|---|---|---|---|
| | time clock, Scan interface | | accelerator (ART Accelerator™) 105 DMIPS/ 1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions Dynamic efficiency line with BAM (batch acquisition mode) |
| UART | 2 | 3 | 3 |
| USB | No | 2.0 | 2.0 |
| Number of I2Cs | 2 | 3 | 3 |
| SPI | 4 | 6 | 4 |
| Number of comparator channels | 16 | 12 | 11 |
| Timers-16-bit | 5 | 4 | 11 |
| Operating Temperature (°C) | -40 ~ 85 | -40 ~ 85 | -40 ~ 85 |
| Rating | Catalog | Catalog | Catalog |
| Cost ($) | 10.17 | 18.23 | 6.18 |
| Lead time | 6 weeks | 6 weeks | 12 weeks |

The MSP430F6659 was the best selection compared based on the parameters provided in the datasheet. The STE32F401CCU6TR microcontroller outperforms the MSP430 series by a large margin in terms of raw throughput and memory availability, however the lead time for the chip was three months which could be a problem considering the limited time frame between remaining to order and fabricate the PCB prototype. The lead time on the MSP430F6659 was approximately six weeks which is more feasible. The additional benefit to using the MSP430 series is the familiarity in the software required to program the microcontroller which is code composer studio whereas STE32F4 series utilize the STM32CubeIDE software. Both programs use C-code so only learning how to navigate the new software, lead time and purchasing a license to access the program are the main barriers shifting the decision to go with MSP430 series. Regarding the MSP430FR6989, this microcontroller is a part of the same family group but is lacking in performance and memory compared to its counterpart. Additionally, the MSP430FR6989 does not have a USB connectivity which would disqualify it from being a valuable option considering a USB to UART connection is mandatory to execute the operations of the system. The goal was to select a microcontroller capable of handling all the required functions demanded by the system without overclocking. Ultimately, the MSP430F6659 was the only option at present that meet all the criteria and constraints and remained in the code composer studio development software which limits navigating and learning an additional software to program the microcontroller.

### 3.2.3.6 Voltage Regulator Selection

| Table 12: Linear, Low Drop Out (LDO) Voltage regulator | | | |
|---|---|---|---|
| Model | TCR3UF33A | TLV70033DDCR | AP2127K-1.8TRG1 |

| Company | Toshiba Semiconductor and Storage | Texas Instruments | Diodes Incorporated |
|---|---|---|---|
| Function | LDO | Linear | Linear |
| Output type | fixed | fixed | fixed |
| Input voltage (max) | 5.5V | 5.5V | 6V |
| Output voltage (min) | 3.3V | 3.3V | 1.8V |
| Voltage dropout (max) | 0.287V @ 300mA | 0.25V @ 200mA | 0.7 @ 300mA |
| Output Current | 300mA | 200mA | 300mA |
| Quiescent current | 680nA | 55uA | 90uA |
| Operating Temperature (℃) | -40 ~ 85 | -40 ~125 | -40 ~ 85 |
| PSRR | 70bD (1kHz) | 68dB (1kHz) | 68dB-54dB(100Hz-10kHz) |
| Cost ($) | 0.40 | 0.48 | 0.37 |
| Lead time | 16 weeks | 6 weeks | 8 weeks |

The voltage regulator selection was limited to the design parameters of the system. The PCB power distribution system would fluctuate as data is received and transmitted through the delay line. Linear regulator would be a poor design selection as it is often inefficient due to the amount of power dissipation. The voltage drop estimated would cause a malfunction of various component because of insufficient power. Additionally, overheating from power dissipation can lead to component failure and RF development which is counter intuitive from all the techniques mentions about PCB design. LDO comparison to linear is necessary to finding an alternative solution to lowering the power distribution beyond what the buck step-down regulators can supply low power to components. Ideally, the Toshiba LDO is a great selection for handling low voltage demands. The main issue is the lead time of 16 weeks for the LDO compared to Texas instrument linear regulator of 6 weeks which produces improved values for lower power distribution. The linear regulator will present design complications that will require altering various circuits to prevent any system failures.

Table 13: Switching Voltage regulator

| Model | TPS61322ADBVR | AP3428/A | TPS62122ADRVR |
|---|---|---|---|
| Company | Texas Instrument | Diode Incorporated | Texas Instrument |
| Function | Step up | Step down | Step down |
| Topology | Boost converter | Buck converter | Buck converter |
| Operating input voltage | 0.9V to 5.5V | 2.5V to 5.5V | 2V to 15V |
| Output Voltage range | 1.8V to 5.5V | 0.6V to 5.5V | 1.2V to 5.5V |
| Output Current | 1.8A | 1A | 75mA |
| Frequency switching | 500kHz – 2MHz | Up to 1.5MHz | Up to 800kHZ |

| | | | |
|---|---|---|---|
| Quiescent current | 6.5uA | 40uA | 11uA |
| Efficiency (%) | 90> | 90> | 96 |
| Operating Temperature (℃) | -40 to 125 | -40 to 80 | -40 to 85 |
| Synchronous rectifier | yes | yes | yes |
| Cost ($) | 0.44 | 0.44 | 1.23 |
| Lead time | 6 weeks | 8 weeks | 6 weeks |

Switching regulators was the optimal choice in terms of safety and efficiency. The problem presented is that the control loop would need to tune accordingly to the system requirements. Solving this problem will require testing in MultisimLive software to verify what additional elements are needed to stabilize the system. Moreover, the switching regulator allowed for more flexibility in handling higher current and larger range of input and output voltages. Feedback resistors, capacitors and inductors will be implemented into the MultisimLive simulation to test and estimate the range of values needed to achieve maximum efficiency in the system. The AP3428/A and TPS62122ADRVR are excellent options for bringing the input voltage of the system with a standard operating voltage range. The final design selection will be determined based on which regulator is able to achieve the highest efficiency. The manufacture standard lead times for both AP3428/A and TPS62122ADRVR was six weeks, hence ordering prior to the end of the semester is ideal to allow sufficient time for PCB assembly. The grating motor power supply will require an additional circuit consisting of a step-up regulator to achieve the 6V demand.

### 3.2.3.5 Power O-Ring Selection

| Table 14: Power O-Ring | | | |
|---|---|---|---|
| Model | LM66100DCKR | MAX40200ANS+T | LM5050MKX-1/NOPB |
| Company | Texas Instrument | Analog Devices | Texas Instrument |
| FET Type | P-channel | P-channel | N-channel |
| Ratio input:output | 1-1 | 1-1 | 2-1 |
| Internal switch | yes | yes | Yes |
| Delay time - ON | 27us | 65us | 1ms |
| Delay time - OFF | 2us | 1.6ms | 5ms |
| Current output(max) | 1.5A | 1.2A | 1.25A |
| Current supply | 150nA | 7uA | 55uA |
| Voltage supply | 1.5V ~ 5.5V | 1.5V ~ 5.5V | 2.8V ~ 5.5V |
| Operating Temperature (℃) | -40 ~ 105 | -40 ~ 125 | -40 ~ 125 |
| Cost ($) | 0.41 | 1.00 | 2.60 |
| Lead time | 6 weeks | 6 weeks | 6 weeks |

The power Oring diode aids in isolating numerous power supplies by functioning as a switch and safety measure to prevent the PCB from overheating due to a faulty circuit. Protecting

against reverse current flow due to a shunt circuit can improve reliability and ensure that the voltage supply does not drop in PCB by a short to ground fault. This is accomplished by blocking output power conversion units and separating the discharged capacitors when a connection is made in the system. Additionally, the FET improves efficiency and reduces heat sink. The major constraint to implementing this system is to check the voltage regulation and verify that it is compatible with the PCB parameters. The LM5050MKX-1/NOPB will not be used due to the delay time compared to the P-channel FETs. Both P-channel FETs are valuable selections for building a protection system for the power supply. Further analysis will be needed to compare the tradeoff between faster delay time and current output.

## 3.2.4 Secondary PCB

In the final iteration of the project, we had two PCBs. One which handled the power supply to the modulator and photodiode and displayed the current progress of the pulse retrieval. The other PCB handled the OSA integration: Sending the start signal to the OSA PCB, moving the motor, retrieving the photodetector signal, sending it to the ADC of the MCU, and sending that data back to the PC to make a spectrum. A diagram of this PCB is shown below.

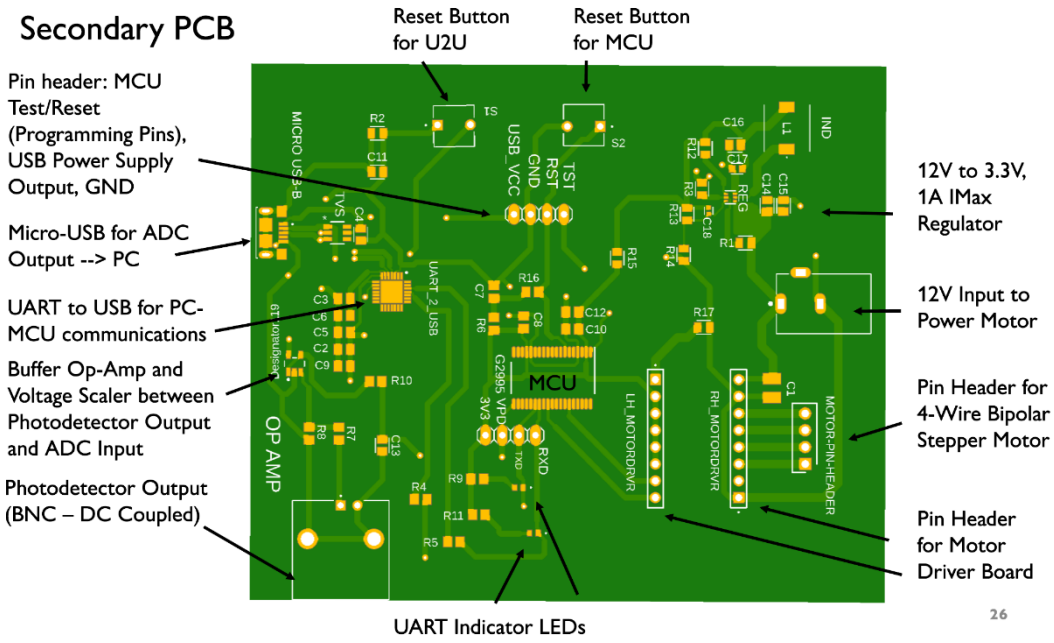



Figure 25: Secondary PCB Layout

The most important part selection for this PCB included the selection of the MCU. The MCU we selected was chosen because it had the least number of pins while still providing the necessary modules we needed (UART, ADC, etc.). Using the least number of pins was important because we assembled this MCU on-campus, and it's easier to troubleshoot IC's when the pins are exposed.

The motor driver board selected which fits into the pin headers on the lower righthand side of the PCB is a Pololu DRV8825 board. This board uses Texas Instrument's DRV8825 Motor

Driving IC but simplifies some connections and only makes the necessary inputs connectable to external circuits. This is important because it saved us time during the design phase as we only needed to utilize basic portions of the operation of the motor driver.

Another important part of the design was the design of the buffer op-amp circuit. This was necessary because in the configuration we had, the ADC could only take a maximum voltage of 3.3V. The photodetector's maximum output when terminated with 50 ohms was 5V with a maximum current of 1 A. This means that not only did the voltage need to be stepped down, but also this large current would need to be separated from the MCU so the pin wouldn't not be overloaded. Thus, we utilized the following circuit to ensure both problems were handled:

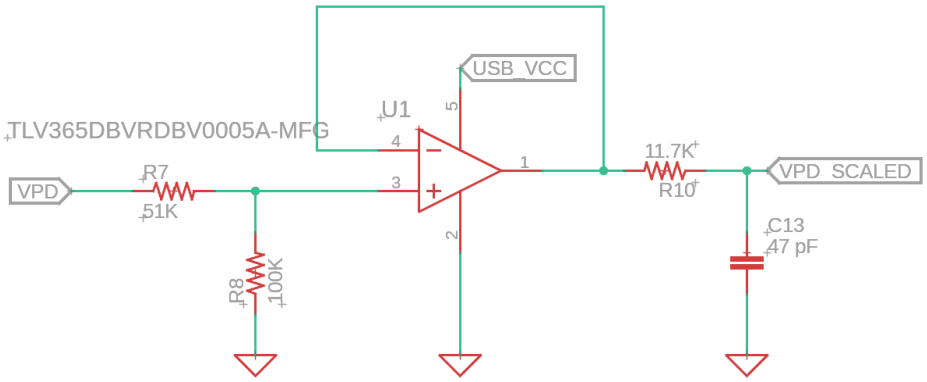



Figure 26: ADC circuit diagram

This shows a voltage divider, which goes into a buffer op-amp circuit, before going into an RC low-pass filter.

Another important aspect of the design was the voltage regulator. We used a voltage regulator to step down the 12V DC, 2A output coming from the wall power supply to 3.3V with a max current output of 1A to be used by the MCU. The design shown was generated via Texas Instrument's WEBENCH.

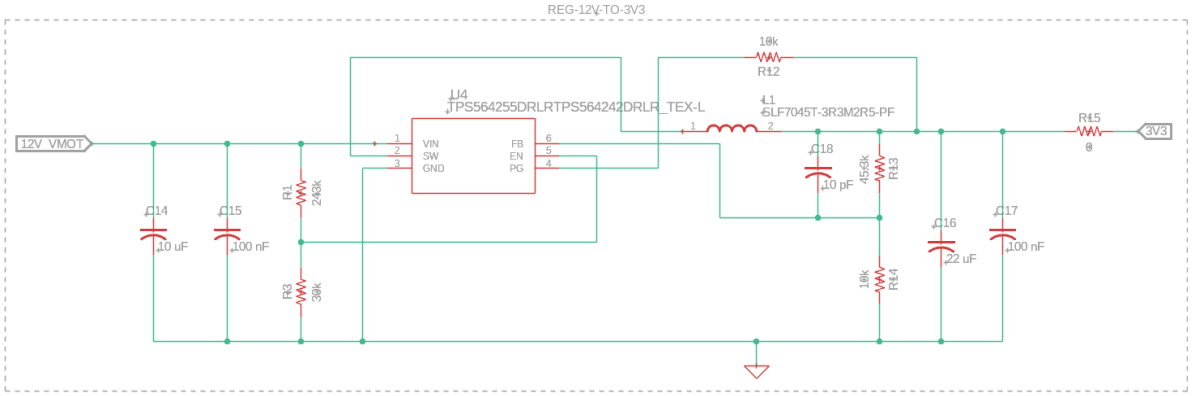



Figure 27: 12 V voltage regulator diagram

There were many other aspects of design on this OSA PCB, but these are the most important subsystems.

## 3.3 Software Part Selection

### 3.3.1 Programming Language Archetype

To develop the computer program which will process the spectrogram generated by the OSA, a programming language must be selected. However, the type of programming language technology to be used must be selected first. Given the high-level mathematical nature of the project, all language archetypes listed are high-level languages. Three different types were compared: object-oriented, scripting, and numerical languages. While the programming language type was selected along with the proposition of the project, it is worth discussing and considering potential technologies that could benefit the project more than the initial selection.

#### 3.3.1.1 Object-Oriented Language

Object-oriented programming languages use classes and objects to organize and access data within the program. This allows for the creation of large-scale programs while ensuring that each aspect of the program has as little dependency on other aspects as possible. Benefits of this include ease of troubleshooting and collaboration and the ability to reuse code through inheritance of classes. While these traits are beneficial to most projects, the development of the FREG program does not gain much benefit as the program is relatively small in scope, aiming to acquire, calculate, and display data to the user.

#### 3.3.1.2 Scripting Language

Scripting languages are mainly non-compiled languages which are easy to learn and quick to modify. These tend to be useful for small, flexible tasks that may deal with different data inputs or need to be frequently modified. This suits the singular scope of the program better than an object-oriented language. However, scripting languages have lower performance and complexity when compared to traditional programming languages. These characteristics are necessary for the FREG project due to the complexity of the FREG algorithm, specifically deconvolution. Scripting languages are also usually extensions of existing programs, which does not lend itself to the creation of a single executable application.

#### 3.3.1.3 Numerical Language

A numerical programming language focuses on using mathematical approximations to accomplish a programming goal, rather than using text or symbols [34]. This allows for more complex mathematical algorithms to be performed seamlessly through implemented functions. Most numerical languages also allow flexibility with input variable types and have significant support for math concepts such as matrices and summations. The FREG algorithm relies heavily on math concepts such as integrals and matrices, so a numerical language provides significant benefits to the project.

#### 3.3.1.4 Comparison & Table

There are four major categories that were used to determine which type of programming language to use: familiarity, accessibility, mathematical functionality, and portability. Familiarity is how much experience we have using that type of language while accessibility is the ease of use and ability to easily learn and use the language. Mathematical functionality represents the amount

of functions and libraries available to perform complex mathematical algorithms. Portability refers to the ability and ease to convert the development files into a packaged computer application.

| Table 15: Comparison of Programming Language Archetypes | | | |
|---|---|---|---|
| | Familiarity | Code Portability | Mathematical Functionality |
| Object-oriented | Used multiple times previously | Completely portable | Has functions in libraries for matrix math, derivatives, integrals, etc. |
| Scripting | Never used | Often not portable | Minimal math functionality |
| Numerical | Used once previously | Partially portable | A large suite of math functions as well as extension libraries |

As shown in the table, we selected a numerical programming language for the FREG project. Numerical programming technology was selected due to the amount of mathematical functionality available, which is very important for the complex calculations and approximations necessary to retrieve the desired data from the laser pulse. The familiarity and accessibility of the other language types would be convenient for completing the project, but the sacrifice of math functions would likely make the project more difficult to program as libraries would need to be found or the algorithms manually coded rather than using a language with integrated functions. The ability to create an executable program for the device would be ideal but is not fully necessary to operate and demonstrate the device.

## 3.3.2 Programming Language

After narrowing the type of programming language to use as a numerical language (section 3.1.1), the specific language and development environment must be selected. Four numerical programming languages were chosen to be compared based on popularity for engineering and mathematical application: Scilab, MATLAB, Python, and GNU Octave.

### 3.3.2.1 Scilab

Scilab has a large selection of mathematical features which include 2- and 3-dimensional visualization, signal processing, and statistics [34]. Tutorials are provided for these features, and basic documentation is available for elements of the code. Scilab is free to use and is open-source, making it accessible and modular for the purposes of the project. While Scilab does not have its own compiler, it is compatible with popular compilers such as Visual Studio. This language is also noted as being compatible with various third-party applications, allowing for more flexibility in the development of the project.

### 3.3.2.2 MATLAB

MATLAB has features including 2D and 3D plotting, data imports and exports, external language interfaces, and a large library of mathematical functions including summations, matrices, transforms, and integrals. This library is also accompanied by detailed and well-organized

documentation, making it easier to use and troubleshoot than other languages. MATLAB is not free, but as UCF students we have access to the software. The main missing feature is the ability to compile into a .exe file, but our group has access to the MATLAB compiler toolbox which allows for this functionality. MATLAB is closed-source, so it cannot be modified for project needs, but it does have multiple toolboxes for added functionality. [35]

#### 3.3.2.3 SciPy (Python)

SciPy is a Python library with a focus on computing complex mathematical problems that use algorithms such as integration, differential equations, and statistics. The library is open-source and free to download and use. The major benefits of this language include its popularity and ease of use, as base Python is extremely widely used and SciPy is a popular library. This means that documentation is expansive and modifications are easy to make. Python also has a large number of compilers available to use, making it easy to package the final product and create an installer. [36]

#### 3.3.2.4 GNU Octave

GNU Octave has standard numerical language tools such as 2-D and 3-D visualization and matrix math. It is also stated to be compatible with MATLAB scripts, making pre-existing code easy to use as a basis, either from Octave or MATLAB. Octave is free to use, but is not listed as open-source. At base, the language lacks some important math features, but packages can be downloaded to expand functionality. The Octave Wiki provides examples and documentation for the language, but it is maintained by a collection of volunteers, not paid employees. [37]

#### 3.3.2.5 Comparison & Table

The following aspects of each language were considered in the group's choice of programming language: cost, flexibility, documentation, familiarity, and math features. As these are all numerically-oriented languages, they all have relatively large amounts of math features. All choices except for MATLAB are free, but MATLAB is accessible to the group, as UCF students are able to use it for free. Flexibility allows for the modification of the code and compatibility with other software, which is useful but not required for the project.

Table 16: Comparison of Programming Languages

| | Cost | Flexibility | Documentation | Familiarity | Math Features |
|---|---|---|---|---|---|
| Scilab | Free | -Open-source<br>-Works with compilers | Basic docs available | Never used | Signal processing, stats, +more |
| MATLAB | Free (for UCF students) | - Only works with proprietary software | Detailed docs for all elements | Used in classes previously | Signal processing, integration, +more |
| Python | Free | - Many libraries available | Detailed docs for base and libraries | Used once previously | Matrix math, integration |
| GNU Octave | Free | -Works with MATLAB | Volunteer-managed docs | Never used | Matrix math, graphing |

As shown in table 16, the group selected MATLAB to use for the FREG project. The primary reason for this selection is familiarity. Specifically, as noted in the related work section (2.4), the Trebino group has created code in MATLAB for the operation of a FROG device. The use of this software as a basis for designing the FREG code is valuable for understanding how to implement the complex algorithms needed to deconvolve the spectrogram into usable data. GNU Octave could be compatible with this software, but the lack of documentation and the fact that MATLAB is free for the group meant that MATLAB was essentially superior in all categories.

Additionally, MATLAB has a built in app developer which can be used to create a GUI. This can be used to build the software used for the FREG spectrogram retrieval process before the deconvolution takes place.

## 3.3.3 Deconvolution Algorithm

To gather the necessary information from the spectrogram, 2-dimensional blind deconvolution must be performed on the acquired spectrogram. 2D convolution is represented by the following equation, where f represents the spectrogram, p represents the probe which is the original laser pulse, and g represents the gate which is generated from the photodiode:

$$f(x, y) = p(x, y) * g(x, y)$$

In the case of 2-D blind deconvolution, both p and g are unknowns, making the process of deconvolution significantly more complex than when a second variable is known. An important principle of convolution is that it becomes multiplication when in the frequency domain. This can be obtained by using Fourier transforms and results in the following equation:

$$F(kx, ky) = P(kx, ky)^* G(kx, ky)$$

Using this information, multiple algorithms have been developed to perform deconvolution, one of which must be chosen to acquire the gate and probe from the spectrogram. [37]

### 3.3.3.1 Principal Components Generalized Projections (PCGP)

The generalized projections algorithm operates as follows: an initial guess is made for the original pulse (the probe vector) by using a Gaussian pulse. Then, the gate function is guessed from the probe vector. The outer product of these two is calculated by multiplying each value of one vector by each value of the other, forming a 2D matrix. This matrix is then row-shifted until it matches that of the acquired spectrogram's time-domain electric field. Finally, the matrix is converted into the frequency domain using Fourier transforms to match or become very close to the matrix of the spectrogram. By matching the spectrogram, the gate and probe vectors can be found from the final matrix, completing the deconvolution. [37]

[38] This algorithm relies on the linear mathematics concept of principal component analysis, which is a method for analyzing large data sets with many facets. It involves breaking down a set of data into principal components and shifting those components to alter the view of the original data set. In this case, the spectrogram is represented as a matrix data set, and the principal components of that set are the gate and probe vectors. The algorithm is also being used in reverse: rather than acquiring the components from the data set, we guess the components to

reconstruct the data set. The ability to use this algorithm for this application relies on the fact that the spectrogram can be constructed using only the outer product of the gate and probe vectors.

The main benefit of using this algorithm is that it has already been adapted for use with FROG systems. Additionally, it is the algorithm used within the FROG code provided by the Trebino group. This means that rather than implementing an algorithm from scratch, the FROG algorithm can be modified and repurposed to work with the FREG system, mainly by removing any assumptions about the symmetry of the received spectrogram. As it has been implemented, the PCGP algorithm is known to function for analyzing a laser pulse and it operates with relatively good performance and accuracy.

#### 3.3.3.2 Linear Prediction

The linear prediction deconvolution algorithm uses smallest-order statistics to perform the deconvolution. This is done by using linear combination, which is an expression consisting of the addition of variables and corresponding coefficients. This can also be defined with vectors and their scalars, which is done for this blind deconvolution. The spectrogram would be defined as a vector with a correlation matrix and correlation vector. An identical vector would then be constructed by guessing the sample correlations which are linear combinations of the spectrogram vector. The identical vector is defined as the inverse of the correlation matrix multiplied by the correlation vector. [39]

There are multiple difficulties with using linear prediction for the FREG deconvolution algorithm. The first is the complexity of the algorithm given the group's limited knowledge of statistical concepts. The formation of a correlation matrix would require additional research of more advanced statistics than are included in engineering course curriculum. The second difficulty is that linear prediction has not been used for pulse retrieval in a published document. The complex math would need to be applied to a spectrogram, which could take a significant amount of research.

#### 3.3.3.3 Higher-Order Statistics Methods

Higher-order statistics can be used to perform 2D blind-deconvolution with methods such as Maximum Normalized Cumulant and Super-Exponential [39]. Algorithms of this type may be possible to use for a FREG system but use advanced math topics. Additionally, they are not known to have been used for any published pulse retrieval systems. As such, due to the complexity of the algorithms and the lack of experience with these math concepts, these methods are unlikely to be used for this project.

#### 3.3.3.4 Comparison & Table

Table 17: Comparison of Deconvolution Algorithms

| | Previously Used for Pulse Retrieval? | Complexity | Group Familiarity |
|---|---|---|---|
| Generalized Projections | Yes | Integrals, differentiation | Familiar with use in FROG code |
| Linear Prediction | No | Matrix math, linear combination | Never used |
| Higher-order stats | No | Complex math; super exponential, | Never used |

| | | | |
|---|---|---|---|
| | | maximum normalized cumulant | |

The choice for the 2D blind deconvolution algorithm is made simple by one key element: the existing use of the algorithm for a pulse retrieval system such as FROG. Using an algorithm that has been used before significantly reduces the amount of research, testing, and development necessary to build the FREG. Given the limited timeline of the project and the limited mathematical knowledge of the group, not needing to figure out a new way to deconvolve a spectrogram is extremely helpful and important. This makes the principal components generalized projections algorithm the best choice for this project. Generalized projections uses matrix multiplication which is a much simpler concept than linear prediction or higher-order statistics as well, so it is the simplest and most proven choice for use in pulse retrieval.

## 3.3.4 PCB CAD Software

Multiple software for designing PCB is available such as Autodesk Fusion 360, Autodesk EAGLE and KiCad.

### 3.3.4.1 KiCad

KiCad is described as an "open source software suite for Electronic Design Automation", including PCB layout. KiCad is free to download and use and does not require an account to download. This program's PCB layout has multiple features listed, including an interactive router for routing wires and avoiding collisions along with a customizable Design Rules Check feature to ensure the PCB meets the desired requirements. KiCad also has the standard features to edit the PCB, schematic, as well as the footprint. It can also import schematics from multiple other CAD programs, including EAGLE, which greatly increases the amount of pre-existing PCB resources. [40]

### 3.3.4.2 Autodesk EAGLE

EAGLE is Autodesk's older PCB design software, and it can only be acquired with a subscription to Fusion 360. It includes features such as electronic and design rule checking, schematic and layout syncing, wire routing, and component alignment tools. EAGLE also has access to a large online library of parts which is constantly updated. As it is a popular tool, it has a large and active community as well as pre-existing articles to help troubleshoot any errors that may be encountered. As it is owned by Autodesk, EAGLE is not an open source platform. Additionally, this program is being discontinued in June of 2026, limiting potential revisions for the PCB in the future. [41]

### 3.3.4.3 Autodesk Fusion 360

Fusion 360 is the newer "unified product development solution" from Autodesk, which can be used for PCB design. It is considered an "all-in-one product development platform", which means it contains extra features for 3D modeling and manufacturing, which will not be used in this case. The PCB design software part of Fusion has similar features to EAGLE: layout and schematic design, routing, design rule check, and a component library. It also adds features related to manufacturing, such as electronics cooling, 3D model integration, and generating assembly files. Fusion 360 requires a paid subscription and is not open-source. [42]

#### 3.3.4.4 Comparison & Table

AutoCAD Eagle is the most familiar software utilized by and would be easy to navigate from past usage specifically in Junior Design. The user's interface was not up-to-date and often frustrating to design in. KiCAD, compared to EAGLE, lacks a wide variety of libraries and certain execution operation essential to designing a high-quality PCB without complication. The only and best solution was to migrate to Fusion 360 which is the newer version of EAGLE with more ways to perform specific functions and an updated user interface. EAGLE and Fusion 360 are normally only accessible with a paid subscription, but as UCF students we have access to the software for free. The only remaining issue present is reserving time to learn and understand the software and all its applications.

Table 18: Comparison of PCB CAD Software

| | Open-source? | Component Library? | Experience with using? | Features |
|---|---|---|---|---|
| KiCad | Yes | No | No | PCB layout<br>Auto-routing<br>Import schematics |
| EAGLE | No | Yes | Yes | Design rule check<br>Layout sync<br>Parts library |
| Fusion 360 | No | Yes | No | All-in-one EAGLE plus manufacturing |

## 3.3.5 SPICE Software

Simulation Program with Integrated Circuit Emphasis, or SPICE, is a program used to simulate electrical circuits. Components such as capacitors and resistors can be placed with modified values to measure output voltage and current, among other features. Many simulators are available, and one must be selected to simulate circuits used on the PCB. Three softwares will be compared: Ngspice, Multisim live, and LTspice.

#### 3.3.5.1 Ngspice

Ngspice is a free and open source SPICE program. It has a number of features including programmability, circuit optimization, and statistical circuit analysis. [43] While these features may be helpful for certain applications, the main focus for this project is on the basic circuit simulation. Ngspice has a basic and dated layout which is not simple to approach. One useful feature that Ngspice has is its integration into Fusion 360 [44], which means that the PCB design and circuit simulation could be used seamlessly without the need to recreate circuits.

#### 3.3.5.2 Multisim Live

Multisim Live is an online circuit simulator which requires an account to use. Being online makes it accessible and convenient, as no software needs to be installed and all of your circuits

can be found on any device [45]. The downside of this is that an internet connection is required to use it. Multisim Live focuses on the basic SPICE features with a clean and easy-to-use interface, but lacks in additional features. An important note is that this software was the preferred choice for most students in circuits labs.

#### 3.3.5.3 LTspice

LTspice is a free simulator available for Windows and MacOS computers. It has a "graphical schematic capture interface" which allows the user to view simulation results and interact with the results through a waveform viewer [46]. The layout is plain and technical, but many tools are included to help analyze the data acquired from the circuit simulation. LTspice appears to have many features, but also a learning curve comes with those.

#### 3.3.5.4 Comparison & Table

While having the fewest amount of features, Multisim Live is the SPICE software that we have chosen for this project. It lacks additional features but maintains the core elements of circuit simulation and result outputs that are needed to verify and troubleshoot PCB components. What makes Multisim Live stand out is the experience that the group has in using it, as it was used previously in circuits classes for design and testing purposes. Ultimately, the additional features of Ngspice and LTspice were deemed unnecessary when compared to the ease of use and familiarity of Multisim Live.

Table 19: Comparison of SPICE Software

| | Features | Familiarity | Accessibility |
|---|---|---|---|
| Ngspice | -Programmable<br>-Circuit Optimization<br>-Statistical Analysis<br>-Fusion 360 integration | Not Used Prior | Open source, free, simple layout |
| Multisim Live | Online storage | Used Frequently | Online access, free for students, simple layout |
| LTspice | -Waveform viewer<br>-Advanced analysis | Not Used Prior | Complex features, free, plain layout |

## 3.3.6 Housing CAD Software

CAD software is also needed to design the housing for the FREG, likely fabricated using 3-D printing. The design is to have the FREG within an enclosure with two ports, one input and one output. The input port would be for the laser source of choice for the FREG while the output port would be connecting the EOM to the OSA. The top of the enclosure will be on hinges in order for easy access to the top of the system for any maintenance. The purpose of the enclosure is for easier transportation of the entire integrated system. The system is fiber based, which can get disorganized fairly easily, however this enclosure can have fiber mounts to loop the fibers around in order to make it more neat. The fiber will be looped around a post inside of the enclosure, but not looped around tight enough to cause dispersion or breakage. The equipment inside the enclosure can also be mounted, that way any vibrations to the table wouldn't affect the setup.

Overall, this design will be altered with adjustable mounts, that way if the components need to be switched around, locking them in won't be an issue.

#### 3.3.6.1 Solidworks

To make the enclosure, the design needs to be created on software that is able to accurately portray the layout. The first one of choice is SolidWorks, which is a 3D CAD software that is used in most industries. The software itself is easy to use, however it does have a high cost to purchase the software. Solidworks is well known for its versatility in 3D modeling for mechanical design. Assemblies in SolidWorks enables us to put together the components of the enclosure into one final product. Using this feature, we can see how each part fits into the mounts and what kind of threading works best for the screws that are available to us.

#### 3.3.6.2 Autodesk Inventor

The other software is Autodesk Inventor, which is similar to 3D CAD software to Solidworks, but this program has more simulation extensions. This enables us to have a visual understanding in how the system works and where there might be stressed spots in the layout. The program itself is free for students, which makes it more accessible for all members. Autodesk is free to use for students, which can be renewed every year as long as the student email is still valid. Autodesk Inventor is mostly suited for 2D CAD drawing and designing. The features enable the user to edit and annotate the 2D drawings. It is also a 3D CAD software that provides professional-grade mechanical designing product tools. Autodesk Inventor and Fusion360 both are from the same company therefore linking and sharing designs interchangeably is fairly simple.

#### 3.3.6.3 Fusion360

Fusion360 is the free version of Autodesk Inventor as well, but the biggest difference between both is their operating systems. Fusion360 is able to run on Apple OS while Inventor is only available on Windows devices. This makes it more accessible by downloading Fusion360 from the website and having everything saved within the account. The design can be transferred and edited from any device and the program is fairly user friendly. Fusion360 also has automated modeling and cloud public shared viewing, which is not available on Solidworks and the user must pay to use these features on Autodesk Inventor. Fusion360 not only has CAD software but also a PCB software platform which makes it more concise to work with within users.

#### 3.3.6.4 Comparison and Table

Overall, while SolidWorks is technically more expensive than Autodesk, the user interface of the program is easier to understand and visually work with. The simulations are strong features of Autodesk that can be utilized to see 2D models of the design. This however is not necessary for a simple enclosure that we want to construct. By seeing the 3D model of the parts and putting them together in the assembly, we can effectively observe how each part comes together to the final design. Fusion360 will also be used when working at other locations from school, however in terms of time efficiency the project will rely on Solidworks.

Table 20: Comparison of CAD programs

| Program | AutoDesk | SolidWorks | Fusion 360 |
|---|---|---|---|
| Cost for Students | Free | $99 Annually | Free |

| | | | |
|---|---|---|---|
| Platform availability | Windows only | Windows only | Windows & Apple |
| 3D Printing capability | Available | Available | Available |
| UI and Tools | Not Available | Available | Not Available |

This comparison table lists the three separate CAD programs that could be used throughout the duration of the project. The listed specifications comparison is just to show what each program has to offer.

## 3.3.7 MCU Communication Protocol

In this project the main responsibility of the microcontroller is to communicate between and synchronize multiple components. To do this, a communication protocol must be chosen which defines the rules used to transmit information to and from the MCU. Our selected microcontroller, the MSP430FR60471 has 3 supported protocols: Universal Asynchronous Receiver and Transmitter or UART, Inter-integrated Communication or I2C, and Serial Peripheral Interface or SPI.

### 3.3.7.1 Universal Asynchronous Receiver and Transmitter (UART)

UART is a communication protocol that operates using two wires, each of which connects to a transmitter port on one device and a receiver port on the other. It is exclusively used between two devices: it has no bus topology, masters, or servant devices. [47] UART is deemed asynchronous because the signals are sent based on the clock within each device, not a synchronized clock between the two. However, both devices must have the same baud rate, which is the number of bits sent over a wire per second, to properly communicate with each other. UART can also be used in half-duplex mode, in which only one wire is used but data can only be sent from one device to the other.

The baud rate of our selected microcontroller ranges from 9600 Hz to 460800 Hz, but also features oversampling which allows the rate to be multiplied by 16. The number of bits sent in a message, the order of bits sent (least- or most- significant first), and flow control can also be customized. To send messages, UART uses a start and stop bit as well as an optional parity bit to keep track of errors.

An important consideration for UART is the compatibility of key devices connected to the PCB. The time-delay line is one such device, which primarily uses UART to communicate. UART also tends to use a computer program such as Tera Term to operate as a terminal, sending and receiving messages to the device through a computer.

### 3.3.7.2 Inter-Integrated Communication (I2C)

I2C is intended for synchronous communication between multiple devices on the same PCB. It uses 2 wires with a bus topology, which connects multiple devices on one bidirectional wire [48]. These wires are called the Serial Data Line (SDA) and Serial Clock Lines (SCL), which transmit the data and synchronize the clock respectively. This topology allows new devices to be added without the usage of additional MCU pins, making it useful for large and complex PCBs with many devices. There are two types of devices connected to these lines: masters and servants.

Masters are devices who can initiate communication and synchronize the clock, while servants idle until communicated to by a master.

There are multiple configurations that can be used for I2C communication. A system can use 1 master and multiple servants, all masters, or a combination of masters and servants to provide the necessary responsiveness for each connected device. The MCU is typically designated as a master and would likely be for the purposes of this project. Each device has a unique 7-bit address to avoid miscommunication, and a distinct register on a device can be a target for the data contained within a message. The MCU being used for the project supports 2 data rates: standard mode which goes up to 100 KHz and fast mode which goes up to 400 KHz. It is important to consider the supported frequency for all of the connected devices on one of the serial buses.

#### 3.3.7.3 Serial Peripheral Interface (SPI)

This communication protocol is full duplex (bidirectional), synchronous, and commonly uses 4 wires. SPI uses a master and servant system like I2C, but there can only be 1 master in this case. The 4 wires used are as follows: serial clock (SLCK), chip select (CS), master out subnode in (MOSI), and master in subnode out (MISO). MOSI and MISO are responsible for transmitting data from and to the master respectively, SLCK synchronizes the clock, and CS selects the subnode that is being communicated to. Chip select is also used to signal the start of communication, when the master "asserts" the subnode that it intends to communicate with. [49]

SPI allows for the connection of multiple servant devices but does not use the same bus topology with fully shared data lines to do this. Instead, it has multiple ways to set up multi-device communication: multiple selection, which is the standard mode for SPI, and daisy chaining. For both methods the SCLK line is shared between all devices. Multiple selection uses multiple CS lines from the master to designate the device that needs to be communicated with. The MOSI and MISO lines are then shared between all devices, meaning that only one device should be selected at a time for risk of corrupting data. The downside of this method is that a CS line is required for each new servant added to the system, limiting the maximum size of a network. Daisy chaining solves this problem by using only 1 CS line shared between all devices. The devices are then connected in a line: the MISO line of the first servant is connected to the MOSI line of the next device rather than back to the master. This continues until the last device is reached, whose MISO line connects to the MISO of the master, completing the chain. This alleviates the need for additional chip select lines but adds to the time it takes to communicate along with not being supported by all devices.

#### 3.3.7.4 Comparison & Table

Each of the communication protocols have distinct benefits, use cases, and limitations which are described in the table below:

Table 21: Comparison of MCU communication protocols

| | # Wires | Max # Devices | Multiple Masters? | Data Rate Range | Amount on MCU |
|---|---|---|---|---|---|
| UART | 2 | 2 | No | 9600 Hz - 460800Hz | 3 |
| I2C | 2 | 128 | Yes | 10000 Hz - 400000 Hz | 2 |

| | | | | | |
|---|---|---|---|---|---|
| SPI | 4 | Theoretically unlimited w/daisy-chain | No | 32768 Hz – 4 MHz | 6 |

The different communication protocols each have potential use cases in the project. UART is ideal for a single component that does not need to communicate directly with other components. That component can also be off of the PCB and physically far from it. I2C has the unique benefit of having multiple masters which can initiate communication between devices, but is not intended for long distance. SPI has a potentially unlimited amount of devices and has the fastest possible data rate, but lacks compatibility and may fail with too many devices. It may also have only 1 master device to initiate communication.

Due to the existence of multiple instances of pins for each communication protocol, all three could be used for different devices in the project. This will greatly depend on the compatibility of each part of the FREG with each protocol and will then fall to the most important requirement for that component: the amount of devices, the ability to have multiple masters, or the data rate. This flexibility is a major benefit of the selected MCU and allows us to design the FREG be as efficient as possible.

For the final design, UART will be used for communication between both PCBs as well as the separate time-delay line. This allows for simplicity and code reuse in the GUI, along with all of the listed benefits of UART. All possible development environments for the MCUs feature UART compatibility, and some can use UART to program their microcontrollers directly.

## 3.3.8 Embedded Software Development Environment

To develop software for both PCBs, an IDE must be used which is compatible with the microcontrollers on each board. Each IDE has its own compatibility, features, and traits which must be considered to choose the best software to be used for the FREG project.

### 3.3.8.1 TI Code Composer Studio

TI's Code Composer Studio is made to be used with TI microcontrollers such as those in the MSP430 line. It has the ability to debug microcontrollers through a USB-FET which is included on most of their LaunchPad products. This allows a developer to start and pause microcontroller software and observe variables, registers, and other information mid-operation. It uses C with additional register-level functions added in through libraries which correspond to each series of MCU. TI also provides a large resource manager which includes many example codes for most of their available microcontrollers. Its main limitation is its restricted use for TI MCUs only. It also suffers from specific register names without any abstraction, which requires significant datasheet searching to ensure the proper registers are set to the right values.

### 3.3.8.2 Espressif ESP-IDF

ESP-IDF is designed for use with ESP32 microcontrollers. It can be installed in a terminal or other IDEs such as Microsoft's Visual Studio Code. It uses Python as its language, with its own libraries that provide register-level functionality. There are examples provided for various functions on multiple ESP32 boards. ESP-IDF also provides a configuration page which allows settings such as baud rate and pin choices to be configured easily through a UI. While functions

are provided, there is not significant documentation provided for how to use and modify them, making development a somewhat frustrating experience.

#### 3.3.8.3 Arduino IDE

The Arduino IDE is intended for use with Arduino development boards and microcontrollers, but has compatibility with others such as the ESP32 line. It uses a C-like language which is unique with its startup and loop functions designed for use with MCUs. Startup is run once when the chip is powered on or reset, and then loop runs infinitely after. There are many libraries already available for use, but community members also make and upload custom libraries for ease of use.

#### 3.3.8.4 Comparison & Table

Having 2 PCBs, each of which with different types of microcontrollers, using multiple development environments is necessary. The comparison of the IDEs is summarized in the following table:

Table 22: Comparison of embedded development environments

| | Ease of use | Compatibility | Familiarity |
|---|---|---|---|
| Code Composer Studio | Somewhat easy to use | TI MCUs only | Used often |
| ESP-IDF | Hard to use | ESP MCUs only | Never used |
| Arduino IDE | Easy to use | Multiple MCUs | Never used |

Ultimately the two selected IDEs were Code Composer Studio for the OSA PCB and Arduino IDE for the FREG PCB. The familiarity with CCS and the use of a TI MCU made it an easy choice for programming the OSA PCB, along with the added features of debugging and large libraries. For the FREG PCB, ESP-IDF was considered but decided against due to the cryptic nature of the syntax and lack of easy documentation. Arduino IDE's ease of use and already created libraries for the intended purpose of the FREG PCB (LCD progress bar) made it an easy selection.

# Chapter 4 Standards and Design Constraints

## 4.1 Standards

Standards are a method for various engineering projects which focus on a topic to have a unified understanding of certain topics or a method by which the projects can be tested and compared. Finding and using standards can be helpful to guide the project's development and answer questions about what should or should not be done in ambiguous circumstances. This section lists standards that may be useful to the FREG project, what information the standards contain, and how they may assist us in completing our project.

### 4.1.1 IEEE-370-2020

The IEEE 370-2020 "Standard for Electrical Characterization of Printed Circuit Board and Related Interconnects at Frequencies up to 50 GHz" provides guidelines about techniques and implementation of high-speed interconnections for fabrication of PCB's up to 50GHz [50]. The

structure of the standard is to establish methodologies of what are the correct way to simulate and measure s-parameters ensuring proper procedures and quality of measured parameters for electrical hardware are followed. The standard defines sets of metric requirements for designing, evaluating, and removing test fixtures and design layout effect through quality and control applications. The document starts off by providing definitions for acronyms and abbreviations regarding various terminology on electronics. The focus is then shifted at exploring common confusion on s-parameter terms and labeling conventions which can be a major issue when looking at datasheet for reference on correct way of labeling components on a PCB layout schematic.

The document proceeds to highlight calibration and De-embedding methods that are useful for establishing reference planes in a design. Precision coaxial connector characteristics regarding expected operating frequencies when analyzing different inside diameter of outer conductor are present for users to use as a based guidelines when considering design techniques. The standard follows up with the different types of s-parameters available and the steps taken to utilize a general procedure of T-matrix manipulation to obtain DUT test fixtures. Next are the criteria for conducting a test fixture design which involves selecting the appropriate de-embedding mode and the process of executing the verification using the s-parameter library.

The following segment dives into ensuring consistency test for a measurement and provides procedures on how to conduct quality design checks. This process involves utilizing instruments for calibrating expected results and measuring accurate output sources to gauge whether the design is good or needs to be adjusted to ensure functionality. The comparison test regarding TDR response and return loss for actual DUT and after de-embedding enabled the user to see theoretical vs experimental results. The scope of the design integration was the last portion which discussed using analytical models and full-wave simulations go gain ideal data and measurements of the system. MultisimLive is the application that will be utilized to asset and calibrate the design faults in the PCB layout. The standard concludes the document with various diagram tutorials and equations as references to use when integrating numerous design techniques.

### 4.1.2 IEEE 2999-2023

This standard is listed as “IEEE Guide for Technical Requirements and Test Methods for Industrial Ultrashort Pulse Lasers”. It describes the parameters that should be tested and listed for all ultrashort pulse laser products, as well as the conditions under which those parameters should be tested. The scope is specifically limited to industrial ultrashort pulse lasers. The listed parameters are as follows: maximum average output power, pulse width, power stability, effective spot diameter, divergence angle, spot roundness, beam quality, signal-to-noise ratio, polarization direction, extinction ratio, pulse power stability, pulse rise/fall edge, pulse rise/fall time, position synchronized output, and environmental reliability [51]. Testing conditions for these lasers are also listed, including humidity, air pressure, air cleanliness, input voltage, ambient temperature, control method, software environment, and test equipment.

IEEE standard 2999-2023 is important for this project as it lists and defines important parameters for ultrashort pulse lasers, which the FREG device is intended to measure. These parameters can be used to determine the necessary parameters to measure and display with the FREG device. If these parameters are measured, then the FREG can be used as a primary or possibly singular tool for testing ultrashort pulse lasers and ensuring that they meet the standard.

Additionally, ensuring that the FREG functions properly under the suggested testing conditions will make the device easy to use as a standard measuring tool.

Important definitions for the project are also provided by this standard. An ultrafast laser under this standard is a laser with a pulse width of <1 ns and >1 ps. This means that the FREG should be able to measure pulses at least as low as 1 ps so that it can be used as a tool for verifying this standard.

### 4.1.3 IEEE 287-2007

The IEEE 287-2007 standard, "IEEE Standard for Precision Coaxial Connectors (DC to 110 GHz)" defines important details regarding precision coaxial connectors, specifically those from dc to 110 GHz. These details include performance requirements, testing procedures (electrical and mechanical), and definitions for precision coaxial connectors. The purpose of the standard is to define minimum requirements for connectors with an 18 – 110 GHz upper frequency and a socket size of 3.5 mm, 2.92 mm, 2.4 mm, 1.85 mm, or 1.0 mm. It also serves to provide testing procedures for each type of connector and has utility as a user's guide to understanding coaxial connectors. [52]

This standard will be useful for understanding, selecting, and testing any coaxial cable connectors used within the FREG device. As the device uses these type of cables, the proper connectors must be selected to connect these cables to components of the device. Additionally, once selected, the test procedures can be followed to ensure that the cables meet the required specifications for the FREG. Specifically, the electrical tests can be used so that parameters including reflection coefficient, connector repeatability, insertion loss, phase, shielding effectiveness, and DC contact resistance are verified to eliminate faulty results due to malfunctioning cable connectors.

### 4.1.4 ANSI Z136.1 (2022)

The "American National Standard for Safe Use of Lasers" gives guidelines for how to use lasers safely for all applications. [53] Specifically, this standard applies to lasers of wavelengths between 180 nm and 1000 microns. Guidelines are given by providing classifications for lasers based on their hazard levels along with instructions for handling lasers at each hazard level. Hazard levels are determined by the amount of damage they can cause to skin or eyes during use. ANSI provides a suggested procedure for the use of this standard: first, determine the class (hazard level) of the laser/system being used. Then, follow the requirements and optionally the recommendations for using a laser of that class. Finally, a hazard evaluation should be performed to ensure that all requirements are met, and to determine any new requirements that should be added or existing requirements removed based on the use case of the laser. The standard also provides important definitions for laser specifications and safety equipment. Additionally, there is an appendix containing a description for the position known as a Laser Safety Officer, who has control over the operation of lasers within a designated region, including the ability to suspend or terminate use of lasers.

The utility of this standard for our project is to ensure that we are following proper safety guidelines when using lasers. To do this, we can ensure that the FREG device meets the requirements listed for its respective hazard classification by following the steps provided in the standard. These requirements should be applied when designing the FREG, building it, as well as

testing it. The spectral range of the FREG is 1-1.5 microns, so it fits within the wavelength specification of the standard. Safety is very important in all stages of the project: design, construction, testing, and eventually production, and the safety of the engineers, committee, project reviewers, and end users of the product should be ensured. Lasers have specific safety concerns that could cause permanent injury that are addressed by this standard, making it particularly vital to consider and use ANSI Z136.

As the FREG is intended to measure low-power and short-pulse-duration lasers, it is mainly intended for class 1 and 1M lasers, which are of the lowest danger level. These lasers only cause notable damage if viewed with a magnification device or other modifying instrument, or by being viewed for a long duration. As such, operation of the device does not require additional surveillance or control measures. Therefore, the main safety precautions to take when using the device with the appropriate laser is to wear laser safety goggles and to avoid looking into the beam for long periods of time. For lasers of this wavelength, overexposure to the eyes can cause corneal burns. To prevent any other visibility of the laser, the FREG will be designed with an opaque housing.

Using low-powered lasers also means that laser-related electrical hazards are limited in danger. However, guidelines should still be followed by grounding all laser equipment, maintaining wires, and covering any electrical ports. Class 1 lasers have no fire hazards, so no additional procedures need to be applied for fire safety.

The ANSI Z136.1 standard is considered a “horizontal standard” for other standards in the Z136 series. This means it contains general concepts and commonly used definitions for all other standards in the series, which are “vertical standards” that expand upon the base information. This is useful for the project as another standard, Z136.8, fits the use case for the FREG device.

### 4.1.5 ANSI Z136.8

ANSI Z136.8 is titled “American National Standard for Safe Use of Lasers in Research, Development, or Testing”. It applies to the same wavelength range of 180 nm to 1000 microns as Z136.1, as this is a vertical standard in the series. It is intended for use when lasers are being tested or researched in testing conditions. This includes use cases in which information about the laser may not be available.

As the FREG is intended for testing lasers, this standard is relevant to the project. Included are definitions for testing areas and restriction levels, guidelines for fiber optic safety, and a warning about extensive working hours with lasers. The fiber guidelines state that fibers should always be treated as if live and that they should never be looked in to, which may be relevant during the design or operation of the FREG. An operator of the device should also be conscious of fatigue to prevent mistakes that could lead to safety hazards. This standard will be followed and considered when using the FREG for its intended purpose of testing.

### 4.1.6 IEC 62129-1 (2016-01)

The International Electrotechnical Commision’s standard for the “Calibration of Wavelength/Optical Frequency Measurement Instruments” has multiple parts, the first of which is for Optical Spectrum Analyzers. The standard’s scope is determined as being used for an OSA used for the measurement of the power distribution of an optical spectrum. The standard includes

information on preparing for calibration of the OSA, including organization, traceability, preparation, and reference conditions. [54] Two different types of calibration are covered: wavelength power level, and calibration is covered for both reference and operating conditions. Additionally, a method for testing the spectral resolution of the OSA is included in the standard.

The FREG device includes an integrated optical spectrum analyzer, so the IEC 62129-1 standard is applicable to the project. Having a standardized method for calibrating and testing our designed OSA will be useful for ensuring that it is functional and accurate. The OSA is a critical part of the project because an inaccurate spectrogram will lead to inaccurate results, making the FREG unusable for serious scientific use. Knowing how to test and under what conditions to test the OSA is essential for completion of this project.

### 4.1.7 IEC 60529 (1989 + A1: 1999 + A2: 2013)

IEC 60529 is a standard concerning the level of protection that a shell around an electronic device provides to multiple entities: protecting people from the parts within in, protecting the electronics from solid objects, and protection of the electronics from water. [55] It applies to any electrical equipment enclosures with a rated voltage under 72.5 kilovolts, which applies to our project. To standardize these levels of protection designations are given to each level, requirements for those levels are defined, and tests are provided to verify that the level of protection is reached. This designation is known as an IP rating, described in the next paragraph.

IP ratings have 2 numbers: the first ranging from 0 – 6 which defines the level of protection against solid objects, and the second ranging from 0 – 9 which defines the level of protection against water. 0 represents no protection while the highest number represents the highest level of protection possible, being dust-tight at 6 and resistant to water at high pressure and temperature. For example, an IP rating of 53 would be protected against dust and spraying water.

The standard also includes methods to protect the shell and equipment within from a variety of external elements, such as corrosion, moisture, mechanical impacts, and solar radiation. Tests and conditions are also provided to verify protection against these elements.

IEC 60529 is relevant to the FREG project as it will have fragile and sensitive components, both optical and electrical, which should be protected from outside objects such as dust and water. This standard can be used to set goals for a desired IP rating to achieve for the housing around the FREG, then test it to verify that IP rating. This is important to preserve the machine given that it uses expensive components to build and would likely have a high cost for a consumer to purchase. While mainly designed to be used in a testing environment, this is intended to be a portable device. As such, it may need to be transported in a vehicle over a variable amount of time, making dust resistance a priority over water resistance. Dust could significantly impact the accuracy and effectiveness of the device, so it must be seriously considered. Defining the system's resilience would ensure that the consumer knows the level of care to take when using and moving the device, as well as the necessary upkeep to maintain the FREG's optical and electrical components.

### 4.1.8 IPC-2221

The IPC-2221 provides guidelines for designing PCBs and other forms of interconnecting structures. The standards document is divided into six sections related to design specifications with detailed instructions on general requirements. Design layout, In-Circuit testing, feasibility density evaluation and performance requirements are some of the followings contained in the general

requirements chapter of the document. A thermal management portion regarding conduction and heat dissipation which is important to consider in any PCB design layout is described in the standard. The chapters provide additional details about interconnections and holes sizes and positioning which is more tuned to board prototyping when dealing with vias and auto routing all the transferred components from the schematic layout. The standards conclude with guidelines on proper documentation principles and ways to design PCB layout correctly for reviewers. [56]

### 4.1.8 IPC-4101

The IPC-4101 on Specification for Base Materials for Rigid and Multilayer Printed Boards provides detailed information surrounding multilayer printed boards and electronic circuits. This standard is important because the design parameters of the FREG system is only possible with a multilayer PCB due to the two USB-to-UART interface integration requirements to form a connection to the time delay line and the PC. The standard dive into thickness tolerance and a slash sheet detailing dielectric properties including loss tangent, surface resistivity and breakdown field strength. Preferred PCB stack ups principles on what to look when searching a manufacturer's capabilities is described in the document. [57]

## 4.2 Constraints

### 4.2.1 Optical Constraints

The optical constraints would be the effects of dispersion throughout the system, we will specifically be looking at 2nd order dispersion. As explained in the optical fiber portion in section 2.2.1.4.3, modal dispersion has a large effect based on the length of fiber and the type of fiber. The length of the optical fiber must be short, but not too short in length or else the laser beam starts to get a halo effect around the center. The halo effect over a laser beam is when the light beam is possibly contaminated with dust particles in the optical path which can scatter the light. Another reason would be nonlinear effects that occur when using high-intensity lasers. The beam profiles become distorted or higher-ordered modes can be generated, which for this project, is not a desirable combination. The light when passing through the cladding is also what makes the beam have the halo look. This is prominent in high intensity pulsed lasers, which we have determined is not a significant concern because the pulse coming in should remain low.

Another optical fiber constraint is the different connectors for all the devices that must be integrated together. Some patch cables have angled polished ceramic fiber end faces or no angled polished end faces. When connecting the fibers, the two different connectors cannot mix at all, or else the back reflections will damage the laser source. Back reflections are when there is optical return loss in which the light will change directions and return into the source. When the power is at its peak, the power of the laser will reflect into the source and cause monetary damages. This constraint is in the single mode fibers because this specific type of fiber is where the problem is most common. There are specialized connectors that must be purchased separately to work around this constraint, however this also adds unnecessary length to the optical fibers. The longer there is in the system, the more dispersion effects are shown in the setup.

The constraints in the polarizing maintaining fibers will be the alignment portion. The stress rods that are in the polarizing maintaining fibers must be aligned together before they can be fully connected or spliced. This is a constraint because this will require a very specific

polarization maintaining splicer machine that is difficult to use and requires a certain technical understanding to function properly.

Another constraint in this system is the previously mentioned signal losses. Due to the motivation of building the FREG, i.e. characterization of low-power pulses, we need to assure that enough of the desired signal is detectable by the OSA. Thus, we must design the beam-splitter power ratio in a manner which optimizes the power which is being used to create the spectrogram. This is a two-pronged challenge, as we want to lose the least amount of optical power to the secondary arm which modulates the main arm's signal, but we still need to properly bias the modulator, so the spectrogram has enough resolution for the deconvolution process.

The system also experiences a constraint in terms of time synchronization between the TDL and OSA. The time synchronization between these two components is necessary because the OSA needs to know when the TDL has been adjusted in time delay before it takes its next recording. Additionally, to create the spectrogram, the OSA needs to communicate with the TDL and record the time delay which has been set on the TDL. We plan to remedy this concern via the usage of a microcontroller with a program on it which automatically increases the delay and signals the OSA to take a measurement of the FREG output.

The spectrogram acquisition constrains the selection of the gate for this system and time delay length. Specifically, the gate period and the repetition rate of the source can be different as long as one of the periods is an integer multiple of the other. Additionally, these periods must be comparable in magnitude. Then, the time delay must be scanned for the longer of the two periods. These guidelines for design are outlined in the original FREG proposal paper. This constraint is also an advantage of the FREG to some extent because it reinforces that the FREG is able to characterize high-bit rate sources without the need of a modulator/gate with the same speed. However, this absolute of the FREG design is a major crux of our design as we investigate how to build an accurate spectrogram. This constraint builds into the overall concept and obstacle of achieving proper pulse overlapping in the FREG, as the gate and pulse periods will play a large role in this. A portion of the gate design will involve biasing the modulator at its point of lowest output power, which can be obtained by first characterizing the modulator and producing a voltage swing curve for input voltage and output power.

Another constraint to the optical design was that we could not find bulk MZMs which had an electro-optical bandwidth larger than 40 GHz. This bandwidth was a limiting factor to the operation of the FREG. This is because the operating bandwidth of the MZM and FPD determines the size of the gate, which subsequently limits how short of a signal we can characterize. We were able to find fast photodiodes with electrical bandwidths which ranged up to 60 GHz, so if we were able to find a MZM with a higher bandwidth, we would then be limited to a 60 GHz operating bandwidth.

The FREG cannot characterize non-periodic inputs. This is why it lends itself to being most useful for the characterization of ultra-short pulse trains, which are inherently periodic. This constraint limits the versatility of the FREG to some extent, which is partially why it is used to characterize these sources before any modulation of the signal has been done in terms of information encoding.

### 4.2.2 Hardware Constraints

#### 4.2.2.1 Delay Line USB Connectivity

A major limitation investigated for the FREG system was the interface connectivity between the delay line and the MCU. The delay line has a built-in USB 3.0 cable which illustrates that a standard USB port is required to enable a compatible connection to the PCB. A USB-to-UART bridge design integration must be implemented to allow the delay line to communicate and transmit data both ways. Multiple bridge connections will be established as one for the delay line and the other for the PC. The port will be configured to a USB 2.0 interface as the baud rate specifications for the delay line are within the parameters for USB 2.0. Additionally, finding a MCU compatible with USB 3.0 was not feasible without changing the development software leading to extending the time of the research and implementation phase to learn and navigate the new software. Selecting a familiar MCU such as the MSP430 series or ATMEGA16U2 chip was the ideal route for reducing complexity of switching over to a new chip with a different development software. All the chips component researched were only USB 2.0 compatible which incentivizes integrating USB-to-UART bridge connections necessary to meeting the system's expectations.

#### 4.2.2.2 Multi-layer PCB

The multi-layer PCB design implementation became the baseline system's requirement when high-speed components were needed to create a communication link to the microcontroller. Fabricating a 4x4 PCB consisting of all the required components and the associated routes for traces and ground would create a disparity in impedance level leading to RF development. Separating the components and routing connection in two planes drastically reduced the risk of running into error during the prototyping phase. Additionally, the trace width and length restrictions are severe and allow for more flexibility in positioning all necessary components on the board. Various techniques are vital for achieving the desired PCB that is fully functional within the FREG system only possible by using a multi-layer design.

### 4.2.3 Software Constraints

A key constraint in the software portion of the project is the possibility of FREG asymmetrical spectrograms. Traditional FROG spectrograms are deconvolved using second-harmonic generation, which assumes the symmetry of a pulse. Second-harmonic generation is a non-linear optical effect, where two photons of the same frequency interact with a non-linear material and "combine" to create a photon with double the frequency of the original photons. [58] The lack of non-linear optical pulse mixing, and thus SHG in the system, means that a different solution may need be found to properly interpret the asymmetric FREG trace.

Another software constraint is that the program must be able to compute the FREG trace and produce the output in under 10 minutes. This is because the device is intended for immediate use, not long-term processing and analysis. The main component causing this constraint is the MCU, as its processing power is likely to be significantly lower than that of the connected computer's processor.

For the code flashed to the microcontroller, the amount of power that it consumes is constrained by the maximum power throughput of the cable which connects the FREG to the computer. As such, the software must use the low-power mode available for any clocks that are

used. This ensures that power will not be used passively for no reason, which could potentially disrupt the function of other components.

The microcontroller's programming is also constrained by the specifications of the selected unit. The MCU we selected has 4 UART channels, which restricts the code to using at most 4 channels for communication. The same is true for I2C and SPI, which our MCU has 2 and 4 channels available respectively. Inversely, the available protocols for the components restricts the protocols that can be used. The selected time-delay line can only communicate using UART, so that must be activated and used on our microcontroller to make the system work. The compatible data rates for components also applies in the same way, constraining the operating speed of the system by the rate at which data can be sent to and from the microcontroller from connected components.

## 4.2.4 Safety Constraints

The FREG system involves lasers and electronics, meaning that there are important safety concerns that must be accounted for. This is split into two parts to address each element of the FREG: optical and electrical.

#### 4.3.2.1 Optical Safety Constraints

The main optical safety concerns come from the use of a laser in the operation of the FREG. The system must be designed in a way that minimizes the risk of eye damage and burning from the laser. The ANSI standards Z136.1 and Z136.8 provide guidelines for defining the hazard levels of laser systems and the measures that should be taken to use systems of each hazard level safely. The range of wavelengths that our system measures is 1 – 1.5 microns, lasers in this range are considered hazard class 1 or 1M, the lowest hazard levels for any laser. The only danger in using these lasers is the possibility for eye damage when the laser is looked in to for prolonged amounts of time. The key design constraint that come with this hazard class is to build an opaque housing around the optical equipment to prevent unnecessary exposure to the laser. For operation of the device, standard safety glasses should be worn and the laser should not be looked directly at.

#### 4.3.2.2 Electrical Safety Constraints

The FREG uses electricity to power the PCB and multiple components, meaning that safety concerns arise. The main concern is avoiding potential electrocution events which might damage the user or the device's components. The IEC standard 60529 defines design elements of housings which provide different levels of dust and water protection to electronics within. The FREG is designed to primarily be used within a sheltered indoor testing environment, but is also intended to be portable. As such, it should have some protection from elements but does not need to resist significant force. Based on the IP scale, a housing with at least level 1 dust and water protection must be designed to ensure the safety of the components within. This would prevent solid objects of 50 mm diameter or greater from entering the system to help prevent fires or other possible damage due to objects within the system. For water, this would protect the system from drops of water which fall vertically on to the FREG, helping to prevent damage from light rainfall or minor wet spots.

Another electrical safety constraint is ensuring that the PCB is designed to handle the maximum required load of all of its connected components. If a system were to become overloaded

or strained with power, important components such as the power supply could be damaged along with damage to the PCB. The system could also be prone to overheating, which could damage components or potentially damage users, especially when considering sensitive components like capacitors.

### 4.2.5 Time Constraints

The FREG project has a limited amount of time in which it can be completed, including certain parts that must be finished before other parts can be constructed and/or tested. A lack of proper time management could result in the incompletion of the project as well as having academic consequences for the group members, including class failure and inability to graduate unless the class is retaken.

The main time constraints involve the academic process at the University of Central Florida. Senior Design 1 and 2 must be completed in consecutive semesters for one project, with the complete fabricated design due at the end of the second semester. Semesters last 16 weeks, giving 32 academic weeks to complete the project along with 5 break weeks, giving about 37 weeks of time to deliver all project requirements. This means that the project must be completed in a time-efficient manner which prioritizes the most important design aspects before ancillary ones. Key components include the FREG system's optical and electrical systems, the embedded software to operate the FREG, a rudimentary version of the PC software to process the FREG trace, and the diffraction grating for the optical spectrum analyzer.

Other time constraints involve the necessary order of events taken within the project, also known as bottlenecks. A major bottleneck is part ordering, which must take place after part selection but before physical design and testing. Multiple parts have lead times of 2 weeks or more, making it imperative to select and then order these parts close to the end of the first semester so that the design can be built and tested during the second semester. All of the components must be considered in this way, as the project's completion depends on the component which is received latest.

### 4.2.6 Economic Constraints

Another design constraint on the project is the cost of components. If the right components are not acquired due to an inability to afford them, then the project cannot be manufactured and tested as is required in senior design. As such, the cost of components is a very important element to consider when selecting parts and designing the FREG. The advisor for this project, Dr. Blanco, has provided the necessary funding for the components of this project. However, this is not a corporately sponsored project and there is not a set budget limit. Dr. Blanco is willing to provide what is necessary to complete the project, but this does not mean that the budget is unlimited.

Multiple important components of the FREG have costs of more than $100. The primary expense which cannot be avoided due to performance requirements is the fast photodiode. As it must have a high frequency, a lower cost photodiode is around $4000. Other expensive components include the time-delay line around $2000 and the electro-optic modulator around $1000. The total cost of just these components is already greater than $5000 and continues to increase with the sum of the others. It is clear from these costs that limiting spending on unnecessary components is essential, including using resources available to UCF students. Key cost-cutting measures that help loosen these constraints include getting free software licenses and

using expensive equipment available at the university such as a 3-D printer or an optical table for testing.

# Chapter 5 Comparison of ChatGPT with LLMs

## 5.1 Pros, Cons, and Limitations of LLMs

ChatGPT is a generative AI chatbot that uses a large language model (LLM) with the name Generative Pre-Trained Transformer 3.5. The user inputs a prompt or question and the chatbot responds with relevant information or another appropriate response. It aggregates large amounts of data from available sources on the Internet and analyzes patterns in the data to generate these responses to user requests. Other LLM-based generative chatbots exist, such as the new Bing and Bard. In this section, the pros and cons of these chatbots will be compared, along with their limitations.

### 5.1.1 ChatGPT

Pros of ChatGPT begin with the cost: it is free to use the GPT-3.5 version with an OpenAI account that can be made with an email signup [59]. It is also simple to use once an account is made: start a chat window and type in a prompt to get a response. The response tends to be in natural language, with a blend of formality and simplicity that avoids sounding robotic while still being easily understandable. These responses can include acting as a search engine which directly answers questions, writing articles about subjects, generating ideas for creative elements such as names or locations, or to edit existing text. ChatGPT is also accessible through a mobile app, making it very accessible for daily use. GPT-4 is a more advanced version of ChatGPT which is also available which can use images as inputs, take longer inputs, and respond to more complex inputs [60]. This advanced version can also generate images with its integration of OpenAI's DALL-E AI, which could be helpful for creating diagrams for research. For design purposes, a large benefit of ChatGPT is that it can be implemented into projects via an API provided by OpenAI [61].

A major limitation and con of ChatGPT is that it cannot cite its sources for its generated responses. It does not rely on any search engine to acquire information and aggregates that information from a multitude of sources, so it is not possible to provide a defined list of references. This is a major detriment for using ChatGPT in research and writing, as listing references and sources of information is essential for avoiding plagiarism and copyright issues. Another limitation is that GPT-4 requires a paid subscription to use, making its additional features less accessible. This means that the base version cannot generate or input images and has more limited use in terms of editing text or completing more complex tasks. ChatGPT is also limited by its recency: it is only trained up to January 2022, so very recent information cannot be acquired through the chatbot.

OpenAI has also listed limitations of ChatGPT on their website. This includes a major issue in which the bot can generate answers that sound correct but are actually untrue. This limits the trust a user can have in the responses generated for research, questions, or fact-checking. The bot also has an issue where it may give different answers for small rephrasing of the same question, which leads to potential unreliability. Additionally, the chatbot does not ask for clarification from

the user for inputs that could be interpreted multiple ways, which would improve reliability and ease of use if implemented. On the other hand, ChatGPT's responses can become repetitive and formulaic in their responses which is a minor issue for research use but a much larger issue for creative and generative uses [62]. The final limitation is that inappropriate requests and responses can still be made, even with filtering. This could lead to misuse of the bot and ethical concerns with it, including the possibility of requiring additional user identification such as a minimum age to prevent malicious or otherwise harmful use of ChatGPT.

### 5.1.2 New Bing

New Bing is a generative AI chatbot, not to be confused with the old search engine. It can be used in the same way as ChatGPT: to ask questions or prompts which provide answers or generate content. This integrates the old Bing search engine into it, which has the major benefit of allowing the bot to cite and link the sources that it uses [63]. This is very significant when using the bot for research purposes to avoid plagiarism. Bing is also free to use with a Microsoft account and can be used on mobile devices by downloading an app. This AI can also be used in Microsoft's Skype chat program, allowing for quick communication of AI-generated answers in a group setting. This chatbot allows you to select a "conversation style" from three options: creative, balanced, and precise, which tailors the type of responses gathered to that style. A major pro of Bing is that it can create images when in creative mode, as well as take images as query inputs. The new Bing is connected to the Bing search engine, so it is not limited on the time for which it can acquire information. As such, it can be used for current-day research and news information, which can be helpful for emerging technologies.

The limitations and cons of Bing are similar to those listed on ChatGPT's website. This is because Bing runs on OpenAI's GPT-4, and its image generation is powered by DALL-E 3. As such, the main limitation is that not all responses provided will be correct, as they are sourced from various parts of the Internet. A key limitation of Bing is that each "conversation" with the bot has a set limit for the amount of inputs that can be made. Therefore, the amount of context that can be acquired from Bing is severely limited, forcing new conversations to be formed that must re-establish any context from a prior one.

Inappropriate responses can also appear on Bing, even with attempts made to filter it. Similarly, due to seeking to avoid inappropriate responses, some information may be censored accidentally, resulting in limited reliability on information, especially on sensitive topics. Syntax issues can also arise, causing varying and unreliable responses, and responses can become formulaic due to the training required for the bot to function as intended. An additional consideration for this chatbot is that Bing is produced by Microsoft, which has interests as an entity in selling their products. As such, answers that are given may intentionally favor Microsoft products or services over other products that may serve the purpose better.

### 5.1.3 Bard

Bard is Google's LLM generative AI chatbot, which is free to use with a Google account and that runs on the LaMDA LLM [64]. As it is tied to the Google search engine, it can cite sources for research questions if prompted to. It can also find current information without any time limitation, helpful for researching on current-day topics. There is also no limit on the number of messages that can be sent in a conversation with the chatbot, allowing the user to continue without the inconvenience of opening a new conversation every few messages. One pro

for users of Bard that also use their Google accounts for other services is that Bard can interact with other Google services such as maps and YouTube to tailor the experience based on your interaction with the other services. Additionally, it can connect with editors such as Docs and Gmail to quickly answer questions or make edits by scanning documents or emails and generating an appropriate response. Bard is listed as being available in over 40 languages and that more languages are being added. This makes the chatbot accessible to a large amount of people across the world and opens up the concept of being able to acquire information from papers and sources in any language.

Bard shares many limitations with other LLMs, including that responses are not always correct despite the AI presenting them as such. Google also purposefully limits the context for conversations, making it so that context must be reset and re-established for long strands of continual conversation, however this doesn't require a reset for the full conversation. This LLM cannot generate images, limiting its generative use, especially for creative purposes. However, it can take images as inputs alongside prompts or questions related to the image. There are limits on the images it can receive: the maximum dimensions are 1024x1024 pixels, the image must be a jpeg, png, or bmp, and the image must be clear and not have any small changes which would throw off the AI's analysis (according to Bard AI). Bard is also not available on mobile devices, limiting its accessibility. While available for many languages, not all languages have all of the Bard features that are available in English. A final limitation for Bard is that users are required to be at least 18 years old.

### 5.1.4 Comparison of LLM Chatbots

All of the LLM chatbots researched in this section have similar basic features and purposes: entering a prompt or question and receiving a response in natural language from the chatbot which aggregates information from a large network of sources across the Internet. They also share the major drawback of occasionally providing incorrect information, which seems to be a continuous issue with all LLMs. In the same vein, each chatbot can produce inappropriate results which is another issue that is constantly attempting to be fixed and requiring indefinite maintenance. Additionally, all of the compared LLMs have basic versions available for free with the creation of an account with its respective website.

In terms of features and performance, ChatGPT with the GPT-4 upgrade has the most due to the image processing and generation as well as the improved capacity for context. However, this is the only chatbot that requires payment to access, providing a significant barrier for many consumers. Bing does use GPT-4 for free, making it the highest-performing LLM for the lowest cost, though it lacks additional features that the upgraded ChatGPT has.

For free versions, the LLM with the most useful features depends on the intended use for it. For research purposes, Bing and Bard are generally more useful due to the important ability to cite sources for the aggregated information. Their connection to a search engine allows this and helps for researching information and asking questions in general due to the ability to access information up to the current day. Both also have the ability to upload images as queries, expanding the possibility for creating captions, finding similar images, or learning information about that image. The main advantage of Bard over Bing for research is Bing's limit on the amount of messages that can be sent in a conversation: this could cause a loss of productivity when researching complex and multifaceted subjects that require a series of queries. Bing may make up

for this in its mobile app access, which can be useful on projects that require travel or for users with a tight and travel-heavy schedule. Both have integrations with other apps to improve productivity as well.

ChatGPT's lack of citing sources heavily limits its research use, but it does have other benefits for generative purposes. The API provided by OpenAI allows it to be integrated easily into projects, which could have important uses in technology related to data searching and organization, for automated customer support, and others. Additionally, the output from ChatGPT is specifically mentioned as being owned by the user: this freedom allows for the potential to create without risk of legal trouble from a large corporation.

Based on the comparisons listed, Bing would likely be the most useful in developing a Senior Design project, with Bard as a close second. Citing sources is very important for this project, so ChatGPT is quickly eliminated with this limitation. The choice between Bard and Bing would likely come down to project details and user preference. Bing's mobile availability may be useful to some groups, but essentially useless for others. The same can be said about Bard's Google integrations, which are useless for a project in which the members are not using Google applications for development.

# 5.2 Effects on Senior Design

LLM chatbots are a recent innovation with lots of features that have not been seen before by the general public. The key difference with this is that content can be automatically generated and phrased using natural language, and that large amounts of information can be aggregated from multiple sources automatically, effectively creating a new "source". This can have a variety of positive and negative effects on the Senior Design learning experience, multiple of which will be discussed in this subsection.

## 5.2.1 Benefits and Detriments of Information Access through LLMs

A key feature of LLM chatbots is that they can provide quick access to aggregated information on a variety of topics, including more advanced engineering topics. For Senior Design this has major benefits, particularly in the research portion of the project. For this project, a chatbot could be helpful for a non-photonics team member to learn about topics such as convolution, deconvolution, and so on. It could also be used in part selection and ordering to find out where to buy optical components or what features could be helpful on certain components. The key improvements of this over a search engine is the ease of use and accessibility. Rather than needing to search and click on a number of different links, some of which may be riddled with ads or locked behind paywalls, the chatbot will provide a small summary of the requested information.

The main danger of using generative AI to gather information for senior design is the potential for incorrect information. As discussed in the previous section, all LLMs can occasionally "hallucinate", responding to a request with incorrect information while claiming it to be the correct information. This heavily limits the ability to use an LLM as the sole source of information, as learning the wrong details could cause faulty design early in development that could later cause significant issues that may be too late to fix. However, this does not prevent the use of an LLM as one source to be compared with other sources.

Another key issue with using ChatGPT specifically for the project is that it cannot cite its sources. This makes it almost impossible to use for Senior Design or any research, as referencing sources is essential for avoiding plagiarism. However, Bing and Bard's connections to search engines do support citations, making them much more applicable for use in Senior Design research.

One concern for the learning experience of Senior Design is that the accessibility provided by generative AI may leave students short-handed in learning how to research without the aid of AI. If for some reason in the future this technology becomes unavailable to use in a project environment, students won't necessarily know how to properly do research via books, websites, or other sources. This could cause an over-reliance on certain technologies that could negatively impact students in the future.

### 5.2.2 Benefits and Detriments of Text Content Generation by LLMs

The other major element of a generative AI is that it can generate content that appears as if it could have been produced by a human. This includes writing articles, editing text inputs for different phrasing, and creating any other form of written communication. This presents a number of opportunities as well as concerns for any written article of text, including the Senior Design project.

One example of a way this generative ability could be beneficial for the Senior Design learning experience is using it exclusively for editing and formatting text. This could be helpful in organizing a paper, fixing grammatical errors, or assisting in using good writing techniques. This is especially useful for people who struggle with writing in English, where some translations can be erroneous even if they seem like they would be correct.

The concerns with text content generation using an LLM chatbot are significant. The key concern is the potential use of these bots to write portions of or an entire paper instead of the student. If used this way, the learning experience of Senior Design is severely diminished, as practicing technical writing and paper organization are essential parts of the project. It also has ethical concerns as to what is considered original content: is a paper written entirely by AI under someone's instruction, should it be considered that person's work? For Senior Design, this is limited to 7 pages because of this. Similar to the research element of LLMs, over-reliance on generated content could harm students' futures in the workforce. Being unable to communicate effectively without the help of a bot makes certain tasks take much longer and would likely be questioned by a manager.

For the quiz portion of Senior Design, generative AI has no particular effects due to the quiz security extension required to complete them. However, for other online examinations with less security, the ability to research questions quickly and specifically could raise concerns on the effectiveness of the exam. In that case, learning ability is severely impacted as students can rely on quickly-accessed and properly generated content that may be hard to check for plagiarism.

### 5.2.3 Benefits and Detriments of Image Generation and Analysis by LLMs

Image generation is the least impactful feature of generative AI on Senior Design. Due to the limitations of AI, it is difficult to generate diagrams and other useful images through the chatbots. As such, it is neither a benefit nor detriment to Senior Design.

Image analysis does have some utility for the learning and research portions of the project. When learning information with complex diagrams, such as circuit diagrams, using an LLM to break down the elements of the diagram could be helpful. However, the same concerns as with text research arise with the potential for incorrect information. Analysis can also be useful for organization of the paper as captions could be generated for images within the text. It is important to note that those captions are created by AI and to check their validity, as with other uses for the chatbots.

# Chapter 6 Hardware Design

## 6.1 FREG Design

As previously mentioned, the FREG design involves several aspects: Tuning of the pulse overlapping, design of fiber lengths to minimize dispersion, and design of the beam splitter power ratio to ensure that there is enough optical signal to resolve the desired pulse characteristics. From previous papers on the FREG, we gather the following design conditions which will contribute to the successful overlapping of the primary and time-delayed pulse.

We first begin by reviewing "Simultaneous temporal characterization of telecommunication optical pulses and modulators by use of spectrograms" by Christophe Dorrer and Inuk Kang. Our first design condition is with regards to the pulse train repetition rate and the modulator's operating bandwidth. Because the pulse train and gate are periodic, we are able to produce a spectrogram. If the signal were not periodic, i.e. random, we would not be able to characterize it with this method. The pulse and gate signals can either have matched periods, or one's period must be an integer multiple of the other. For the former case, the delay is scanned for the period of the signals, since they have the same duration. In the latter case, the delay must be scanned for the duration of the larger period.

For example, our test laser has a repetition rate of 50 MHz. It is unideal for us to use a 50 MHz modulator, as that severely limits the abilities of our system. However, our selected modulator or gate is 50 GHz, which is an integer multiple of the pulse signal. Thus, we can characterize the pulse train. Alternatively, if our pulse train was still 50 MHz, and the modulator was only 10 MHz, we could still characterize the pulse train. The limit to this being that the gate's width must be comparable to the pulse duration to be measured. This means within 1-2 orders of magnitude, as it has been proven that 30 ps gates can be used to characterize 900 fs pulses [65]. This is one of the major advantages of the FREG system, the ability to be able to "characterize high-bit-rate sources with lower-bandwidth modulators". [2] Once we determine that the pulse periodicity and gate periodicity are either matched or multiples of one another, we must tune the spectral resolution of the spectrogram. This may require some trial-and-error.

Typically, the gate width is half of the period of the modulator. Thus, in our case, the gate width would be approximately 10 ps. However, this may vary and can be verified once the deconvolution is completed, as the spectrogram will not only return information on the pulse train but the transfer function of the modulator as well.

From the 2014 paper “Controlling free-carrier temporal effects in silicon by dispersion engineering”, we gather that the electro-optic modulator’s operating bandwidth should be matched to the fast photodiode’s bandwidth. This is because in the configuration we are using, the modulator is driven by the photodiode. Thus, if their bandwidths are not matched, it is inefficient. If the photodiode’s operating frequency is higher than the modulator, the modulator will not respond to the RF input due to the device composition. Specifically, the RF input creates a change in carrier concentrations in the device, which changes the refractive index in the EOM which causes the amplitude modulation of the optical signal. If the device is driven at a frequency higher than supported by its electro-optic bandwidth, this generation and recombination of carriers in the modulator cannot happen as quickly as the RF input is changing. Alternatively, if the modulator’s operating frequency is higher than the FPD, it is pointless, because the RF driving voltage is established by the FPD, thus we are not using the modulator’s full potential. High-frequency modulators are also more difficult to find than high-frequency photodiodes for the range we’re looking at, so it would be a detriment to not utilize that functionality.

The beamsplitter power ratio is another aspect of the FREG design. This will first require characterization of the beamsplitter, followed by a signal analysis to determine whether the output power is adequate. When characterizing a beamsplitter, one of our main concerns was how to differentiate whether inconsistencies in measured output power were due to an error in the splitting ratio or due to losses. For the sake of our characterization, we assumed that the power-splitting ratio given by the manufacturer was accurate and assumed that any losses measured were insertion losses. This was substantiated as the measured losses matched the insertion losses specified by the manufacturer, for the beam-splitter that was characterized for the demo. We will continue this procedure with all beam splitters used for the set-up. Refer to Section X for more information.

To calculate the power ratio, we must first acknowledge our constraints in the system. Ideally, we wish to minimize the amount of power being sent through the secondary arm which will modulate the non-delayed optical signal. This is because we want to lose as little of the optical signal as possible. The system is already low energy, thus, losing the optical signal to the modulating electrical signal is unideal. The more power in the main arm/ reference arm of the FREG, becomes more optical signal which is detected by the OSA and recorded in the spectrogram. This creates a more accurate and detailed spectrogram in terms of range of modulated intensities recorded which makes the pulse characteristics easier to retrieve.

The method for calculating the necessary power ratio relies on finding the minimum possible optical power that can be sent into the secondary arm whiles still achieving FREG operation. This mainly involves summating the various types of losses throughout the optical path, as well as taking into account the photodiode electrical noise and electro-optical conversion losses. However, because the FREG is a characterization tool, we must take into account the following: The average power of the sources being tested will vary, and the losses of the system may vary as the input varies.

To address the concern of the power of the sources being characterized changing, we must implement a way for the user to adjust the system, so they are able to characterize different sources. Our proposed solution is to characterize the losses in the system, and determine which losses stay constant with changes in source and which change. Overall, we know that generally our inputs will have some similar parameters such as wavelength range and spectral width. Thus, we can use what we know will be constant in conjunction with determining the sensitivity of the system to other

factors in the input changing to determine how the system can be adapted for different sources. This will likely require experimental results to understand how to address this further.

In order from the beginning of the FREG to the output of the FREG, the relevant characteristics are the IL, PDL, and RL of the BS, TDL, MZM, and FPD. Additionally, we must consider the sensitivity of the OSA, as this will determine the minimum-power of a signal which can be detected. Both losses and noise can contribute to loss of the desired signal, thus we will also calculate the electrical noise (example: shot noise) of the FPD and determine whether electrical noise is relevant to the minimum expected input power for the system.

# 6.2 Optical Spectrum Analyzer Design

The design of the Czerny-Turner optical spectrum analyzer (OSA) was completed in two phases. We first completed calculations by hand with estimates of the desired performance. We then utilized an optical simulation program called Ansys Zemax OpticStudio, more commonly referred to as Zemax, to simulate and optimize our system before building. The Czerny-Turner configuration is a common type of spectrum analyzer, and thus, there exists pre-established design equations for the system that we will be utilizing. First, we will discuss our pre-chosen performance specifications which must be met by the OSA, go through the design equations, then show the implementation in the design software and the optimizations made.

## 6.2.1 Optical Spectrum Analyzer Calculations

The necessary performance for the OSA for its integration into the overall FREG system was dependent on two main parameters: It's operating wavelength range and spectral resolution. The operating wavelength range is the band of wavelengths of input light for which the spectrum analyzer can analyze and resolve. The spectral resolution is the sampling rate of this operating bandwidth such that we can recreate an accurate depiction of the spectrum for use in the deconvolution algorithm. Along with the wavelength range and the spectral resolution, we also had a target focal length for the mirrors in the set-up, as we wanted the spectrum analyzer to be relatively easy to build. If the focal length is designed to be too small, the distances between components will be >1 cm, which is difficult to build on a typical optical breadboard by hand.

The performance parameter limits were determined via a survey of devices which are like the device we would be characterizing. Below is a table showing the specifications of a few other ultrashort pulsed lasers. We researched 10+ of these devices and utilized the maximum and average values of their parameters to make design determinations for what our OSA needed to be able to resolve. This is because the FREG is a characterization system, meaning that there is a certain degree of variation of the input which will need to be accounted for. The only stipulation was that we were not able to find any other soliton ultrashort pulsed lasers to compare to the laser we used to test our initial design. The main difference between these soliton lasers and a typical ultrashort pulsed laser from an outside perspective, without looking at the internal engineering, is mainly the pulse energy. However, we were given an expected range for the pulse energies which the system would need to be sensitive to. This means that the noise floor and signal losses must not impede the readout of signals with a minimum power determined by this range. Thus, we will use this pulse-energy range and subsequent calculated pulse-power as our reference when looking at sensors such as the photodetector for the OSA.

| Table 23: Survey of Femtosecond Lasers | | | | |
|---|---|---|---|---|
| Model No. | Arche | PL-FM-DCF.. | FPL-01CFF | FML-15-B |
| Company | FYLA | LDPD | Calmar | Optilab |
| Wavelength Range (nm) | ±10 | - | ±2 | ±20-35 |
| Central Wavelength (nm) | 1560 | 1550 | 1550 | 1550 |
| Average Power (mW) | 2 | 30 | 0.5 | 30 |
| Pulse Energy (pJ) | 40 | 300 | - | 1000 |
| Pulse Width (fs) | 500 | 120 | 500 | 200 |
| Repetition Rate (MHz) | 50 | 20-100 | 20 | 10-100 |

We find from a survey of ultrashort lasers, that there is a lot of variation in the spectral bandwidth of these devices. We only looked at ultrashort lasers which were not marketed as high-power and operated with a center wavelength of around 1550 nm. We found that the spectral bandwidth could vary between ±3 nm about the central wavelength all the way to ±35 nm. Thus, we compensated for the maximum of these spectral bandwidths, to assure that our set-up could accommodate a large variety of these ultrashort lasers. For reference, the laser being used to test the system initially has a reported spectral bandwidth of ±10 nm. Thus, this laser is well within the specification of what we are building. Additionally, using the information that the smallest spectral bandwidths are on the order of ±2 nm for these lasers, we need to choose a spectral resolution which can somewhat accurately characterize this. For this, we found the Nyquist Sampling Criterion or Nyquist Theorem to be a relevant metric. The Nyquist Theorem essentially states that to accurately sample a given analog signal to produce an accurate depiction of the signal contents, we must sample the signal at a rate which is more than double its highest frequency component. Thus, the following calculations were performed to determine an acceptable range for the spectral resolution:

We know that a smaller bandwidth will require a finer resolution, thus, utilizing the smallest spectral bandwidth found for an ultrashort laser from our research, we find that the minimum spectral bandwidth (B) is 1 nm.

We can use this information to calculate the spectral resolution via the Nyquist Theorem:

$$B = 1\,nm$$

Converting from wavelength to frequency:

$$c = \lambda f \rightarrow f = \frac{c}{\lambda} \rightarrow 6 \cdot 10^{17}\,Hz$$

The Nyquist Sampling Rate (fs) is double the highest frequency of the signal (fm), thus:

$$f_s = 2f_m \rightarrow f_s = 2 \cdot (6 \cdot 10^{17}\,Hz) = 1.2 \cdot 10^{18}\,Hz$$

Converting back to wavelength, we find the necessary sampling rate of the operating bandwidth:

$$\lambda = \frac{c}{f} \rightarrow \frac{c}{f_s} = \Delta\lambda = 0.25\,nm$$

Thus, we find the minimum spectral resolution required to properly resolve the possible ultrashort pulsed-laser spectrums to be 0.25 nm. However, because this device is an extreme case, and we find that generally the spectral bandwidths were ±10-20 nm, we will allow for a range of 0.1 nm – 0.5 nm for the sake of optimization and buildability of the spectrum analyzer. The lower limit of 0.1 nm was defined because market spectrum analyzers evaluated (such as the Ando AQ6317B) have a spectral resolution of 0.01 nm. Thus, having a spectral resolution 10x less would be a desirable metric to achieve considering this system is being built with less resources than the typical commercial spectrum analyzer. The higher limit of the spectral resolution is double the spectral resolution determined by the calculations shown above. We will see later in the design equations that the spectral resolution will heavily affect the designed slit width for the spectrum analyzer. We see that this resolution range is important, so we have room to adjust the parameters and design a realistic spectrum analyzer.

Overall, we will aim to build a spectrum analyzer with an operating bandwidth of ±35 nm about a central wavelength of 1555 nm with a spectral resolution between 0.1 - 0.5 nm. In addition to this, we desire that the focal lengths of the mirrors used to be around or in the 100-200 mm range as this makes the system easier to build and adjust with the resources available to us. It would also eliminate the need for micrometer or millimeter positioning stages, as 100 millimeters (about 4 inches) can be measured with simpler tools. In addition to this, after researching diffraction gratings which work in the desired wavelength range of 1550 nm, which can be found in Section 4.x.x.x, we found that the typical reflective transmission grating's groove density for our purposes is 600 grooves/mm. We begin our calculations with the assumption that the detector's active area will be 1-2 mm in width. With these parameters defined, we can venture into the process of designing the spectrum analyzer.

Establish Minimum and Maximum Wavelengths

$$\lambda_1 = 1515\,nm \qquad \lambda_2 = 1585\,nm$$

Operating Wavelength Range and Desired Optical Resolution

$$(\lambda_2 - \lambda_1) = 70\,nm \quad \Delta\lambda = 0.5\,nm$$

As previously stated, we know through researching gratings which apply to our operating wavelength range that the grating groove density will be 600 grooves/mm.

We are utilizing the Czerny-Turner spectrometer configuration, which typically has $\phi$ values between 24-30 degrees. This is a degree of freedom within our design. Ideally, $\phi$ is chosen such that the angle of the light incident on the surface of the diffraction grating (α) is equal to the angle which the light is being diffracted off the grating (β). We can now solve for these α and β angles through the usage of the following equations:

$$\alpha = \sin^{-1}\left(\frac{\lambda_c G}{2\cos\left(\frac{\phi}{2}\right)}\right) - \frac{\phi}{2} \;\rightarrow\; 14.3°$$

We put these equations into a spreadsheet and adjusted the value of $\phi$ within the range of 24- 30 degrees such that we could find a suitable value where α=β:

$$\beta = \phi - \alpha \;\rightarrow\; 28.7° - 14.3° = 14.4°$$

Utilizing the information previously established of the detector active area width (LD), we can find the focal length of the focusing mirror (LF):

$$L_F = \frac{L_D \cdot \cos(\beta)}{G \cdot (\lambda_2 - \lambda_1)} \rightarrow 46\,mm$$

Ideally, the magnification of the spectrometer should be as close to 1 as possible [70]. This is because we want to image the input slit onto the photodetector in a manner which limits the loss of optical energy. This magnification is another degree of freedom which can be adjusted in the design if necessary. We can utilize this conclusion about the magnification to then calculate the focal length of the collimating mirror (Lc):

$$M = 1 \qquad L_c = L_F \frac{\cos(\alpha)}{M \cdot \cos(\beta)} \rightarrow 46\,mm$$

With the information found regarding the amount of dispersion due to the diffraction grating (G), the desired spectral resolution (Δλ), the focal length of the collimating mirror (Lc), and the incident angle on the diffraction grating (α), we can determine the width of the input slit/aperture:

$$w_{slit} = \frac{G \cdot \Delta\lambda \cdot L_c}{\cos(\alpha)} \rightarrow 14.29\,microns$$

Thus, we find that this design is relatively viable in terms of the slit width. Typically, we are looking for a slit width above the 5–10 micron range, as the smallest available slits on the market are 5 microns in width. The slit width also serves as a design constraint because if it is too small, not enough energy can propagate through the spectrum analyzer, making the measurement process more difficult or impossible if the signal is obscured by noise.

Because we are utilizing curved mirrors, we can approximate the radius of curvature of the mirrors with the following equation:

$$f = \frac{-r}{2} \rightarrow r = -2f$$

Thus, we find that $r_c = r_F \approx -92.3\,mm^{-1}$. With this information, we can begin a simulation of the system in Zemax.

## 6.2.2 Optical Spectrum Analyzer Simulation in Zemax

We input the optical design previously calculated into the optical simulation program, Zemax. We will be utilizing the sequential ray-tracing mode, as seen by the negative thicknesses, which indicates the non-linear orientation of our spectrometer. In addition to the lens data editor shown below in Table 24, we have input the Object Space Numerical Aperture (NA) of the system to be 0.14 with a Gaussian apodization factor of 1.0. This is because the input to our spectrometer will likely be optical fiber, thus we utilized the parameters of Corning's F-SMF-28 Ultra for the simulation of our set-up. In addition to using the NA of the of the fiber, we also used the core diameter of 8.4 microns to set the clear semi-diameter of our aperture stop, as the slit in the CT spectrometer is replaced by the end-butt of the fiber.

Additionally, we have simulated the output of this device at the extremes of the wavelength range, the desired center wavelength, and intermediate values. Respectively, these values are 1515 and 1585, 1550, 1532 and 1567 nm. This is because we must optimize the separation of wavelengths which are dispersed onto the detector. We will likely need to increase the number of

simulated wavelengths as we get closer to our desired spectral resolution of at least 0.5 nm, to improve the accuracy of our simulation.

Table 24: Lens Data Editor (Post-Optimization)

| Surface Type | Comment | Radius | Thickness | Material | Clear Semi-Diameter |
|---|---|---|---|---|---|
| Object | Source | Infinity | 2.000 | | 1.000E-2 |
| Stop (aper) | Slit | Infinity | 27.000 | | 0.004 |
| (aper and tilts) | Collimating Mirror | -57.740 | -46.625 | Mirror | 12.700 |
| (aper and tilts) | Grating | Infinity | 37.966 | Mirror | 12.500 |
| (aper and tilts) | Focusing Mirror | -68.960 | -47.737 | Mirror | 12.700 |
| Image | Slit Image | Infinity | - | | 1.000 |

Shown in Table 24 is the post-optimization lens-data editor information from Zemax. All values shown are in millimeters. In addition to this information, the lines/um of the diffraction grating is entered as 0.600, and the diffraction order of the grating is set to m=1.

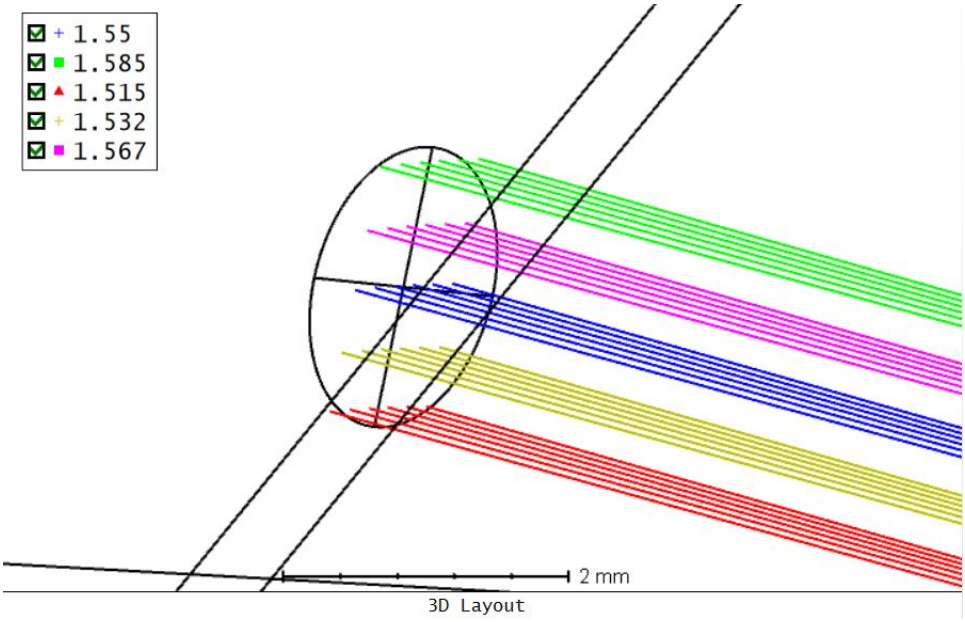



Figure 28: Qualitatively shows how the desired wavelength range is spread across the detector.

This design will require further iterations, as currently the desired spectral resolution has not been achieved. We can see from the images of the simulation, that the current spectral resolution is undesirable as the entire wavelength range (70 nm) is focused onto a plane about 2.4 mm wide. As our detector is 2mm wide, this is not ideal. We will require a span of 0.5 nm of the wavelength range to be focused onto the detector at a time. This means we will need to rework the design to accommodate this design restriction.

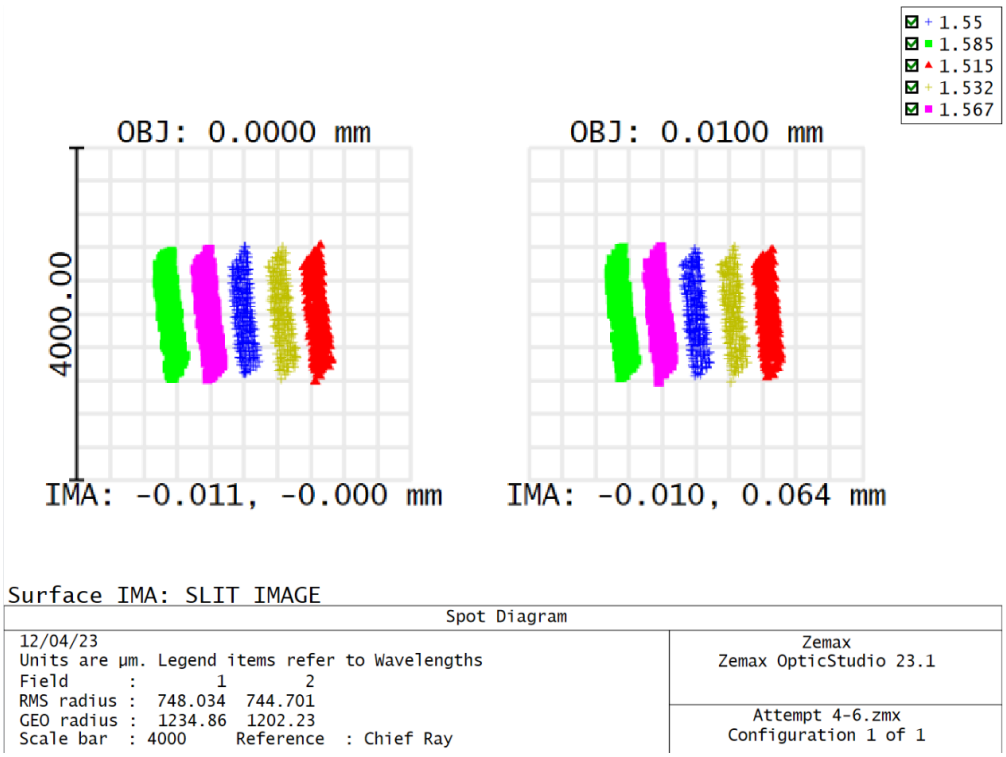



Figure 29: Shows the simulated slit image on the detector, which is the imaging plane. We see that the total region shown is 4000 microns or 4 mm. Thus, every box is 0.4 mm. Because the wavelength range spans ~6 boxes, we have calculated the wavelength range to span 2.4 mm of the imaging plane.

In addition, we find the system has the following parameters in terms of the tilt of the mirrors and diffraction grating:

| Table 25: Tilt of Various Optical Components in the Spectrometer Design | | | | | | |
|---|---|---|---|---|---|---|
| | Tilt Xi | Tilt Xo | Tilt Yi | Tilt Yo | Tilt Zi | Tilt Zo |
| Diffraction Grating | -30 | -30 | 35 | -30 | 90 | -90 |
| Collimating Mirror | 20 | - | - | - | - | - |
| Focusing Mirror | 20 | - | - | - | - | - |

It is likely that these parameters of tilt of the various components will need to be optimized further and taken into consideration for the actual building of the system. This is because typical optical mounts have a limited degree of tilt possible. The overall system is shown below:

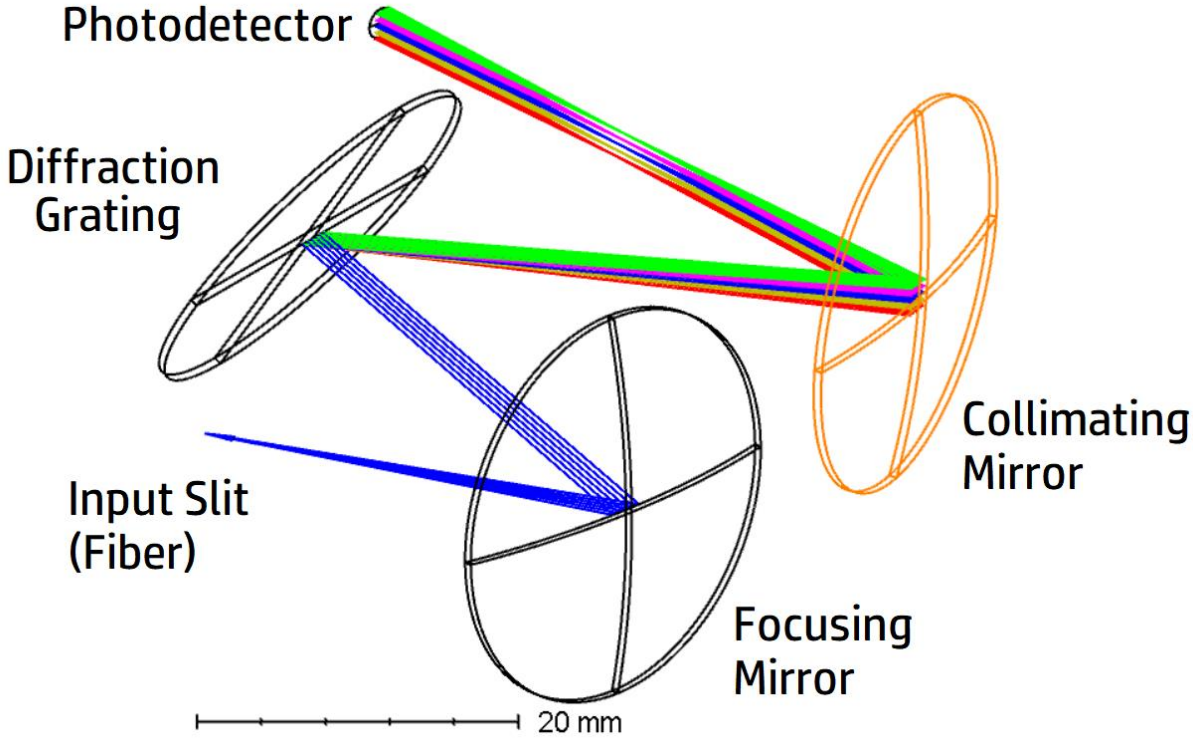



Figure 30: Shows the overall spectrum analyzer design in Zemax, in its current iteration.

To conclude the Zemax design, we note that it is entirely possible to simulate the angle of rotation of the diffraction grating required to image different portions of the optical spectrum of our input light. This is important, because we will have an estimation of the required rotation of the motor before assembly of the set-up, which will make the building process more efficient. However, before this is done, as previously mentioned the system will require further optimization in the simulation program.

# Chapter 7 Software Design

## 7.1 Embedded Systems Software

The PCB contains a microcontroller unit which must be programmed to handle the inner workings of the FREG. The primary directive of the software is to communicate between the components within the device as well as with the connected computer. The FREG PCB communicates with an LCD to display a progress bar for the pulse acquisition. The OSA PCB is instructed to move the motor through a value sent by the PC, then reads the ADC and sends the value back to the PC over UART.

To program the microcontroller, the Texas Instruments Code Composer Studio IDE will be used. This is the proprietary TI IDE for all of their microcontrollers and is used to ensure compatibility of the code with the hardware. Also included in this software are libraries for each family of microcontrollers, including the header file “MSP430.h”, which contains useful functions

for the MCU to perform specific functions that would not be found in base C. These include the ability to set specific registers and to activate low power modes.

### 7.1.1 Embedded Software Flowchart

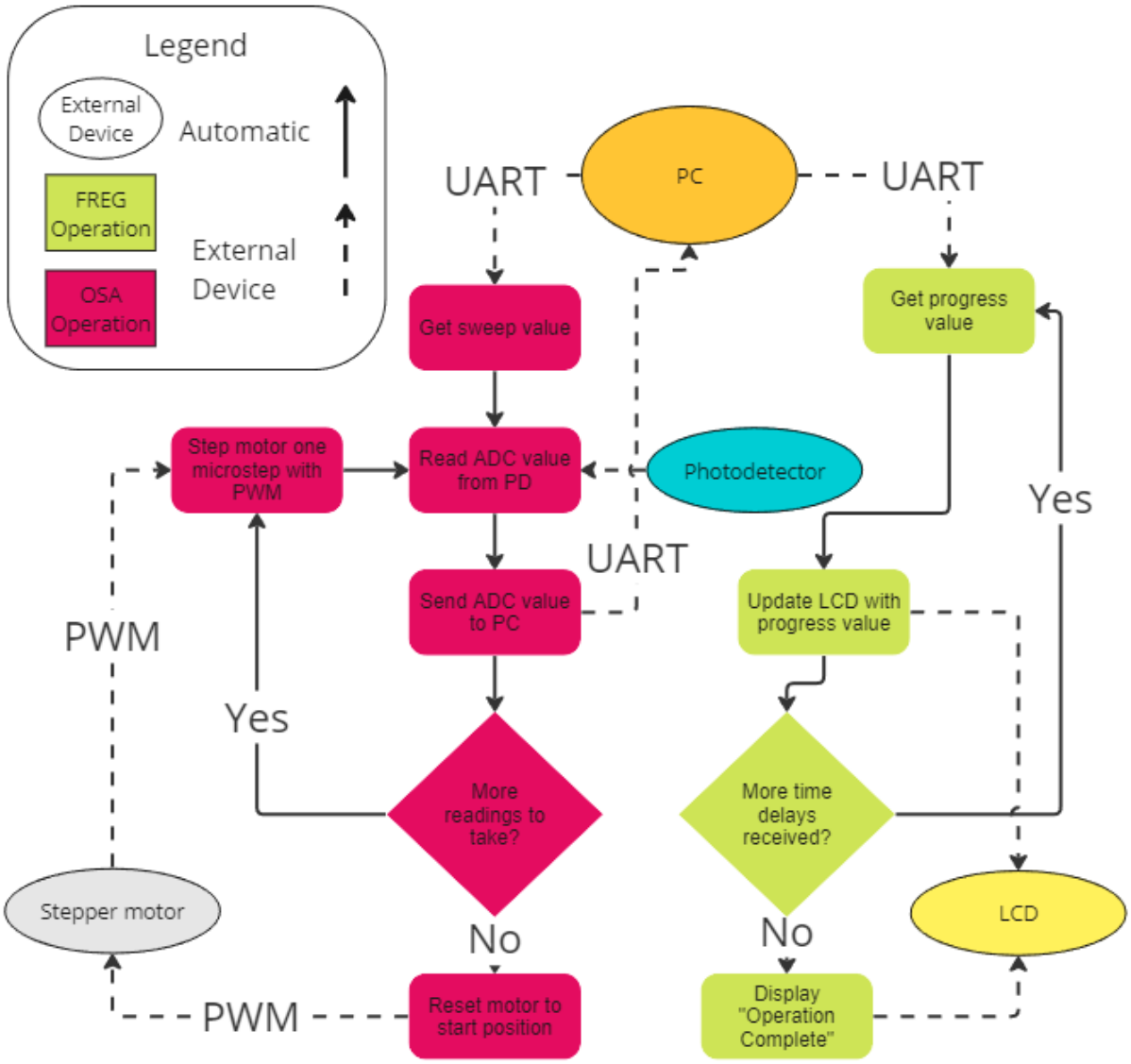



Figure 31: Embedded software flowchart

### 7.1.2 OSA PCB Software

This pairing uses UART as its communication protocol as required by the time-delay line due to its compatibility. The selected time-delays must be sent from the delay line to the MCU using a UART channel. These must then be sent to the computer, also by using UART, in the same order as the delay line is applying to the laser pulse. This will allow for the spectrogram to be properly assembled, which is discussed in section 7.2.2.

To use UART on an MSP430 microcontroller, the MSP430's Family User's Guide document and the MCU's data sheet should be referenced. The family user's guide details the available baud rates for UART and the registers that must be set to acquire that rate. It also has multiple pages which list the relevant registers for UART operation and what they do which allows the programmer to select the necessary settings. The chip's data sheet contains the capabilities of each pin on the chip and what control bits must be sent to use each of the listed functionalities. In this project, 1 UART channel is used to send and receive values to and from the OSA PCB which uses and MSP430.

According to the data sheet of the time-delay line [67], a baud rate of 9600 Hz with no parity, 8-bit data, and 1 stop bit should be used to communicate with it over UART. The family user's guide details the names of these registers, with the baud rate settings being determined by the frequency of the clock used on the PCB. The link with the time-delay line may only require one-way communication from the MCU to the delay line, so only a UART write function would needed for this part in the code. As such, only half-duplex UART needs to be used so only 1 pin must be configured. This pin must have the capability to transmit by containing the "TX" attribute.

To be determined in testing, full-duplex UART may be needed for the time-delay line connection. This is due to the homing feature of the delay line in which the motor within the line must be recalibrated. The need to home is determined by the difference between the signal sent to the line and the signal that is sent back to the MCU. If the system can be set up in a way in which homing will not be needed during the pulse retrieval process, then half-duplex can be used. Otherwise, full-duplex must be used by configuring a pin for transmission and a pin for receiving. In this case the connected computer pin selection of 8.3 would be used for delay-line communication and another pin would be selected for the PC.

To communicate with the connected computer, another pin must be configured to use UART. This receives the time-delay values from the computer which will then be sent to the time-delay line. For simplicity, the same baud rate and data settings will be used as for the delay-line: 9600 Hz baud rate, 8-bit data, and 1 stop bit. This is also a half-duplex setup, requiring only the ability to receive UART messages. A pin with the "RX" attribute must be used.

## 7.1.3 Motor Control & ADC Reading

### 7.1.3.1 Stepper Motor Control Details

The motor within the OSA must be moved with respect to the value of the time-delay line. A common method for driving motors through an MCU is pulse width modulation (PWM), which will be used in this project. PWM is a specific type of signal which has a set window of time that is used as a reference for the strength of the signal. The strength is determined by the amount of time in which the signal is high compared to the length of the time period in percentage. This percentage is known as the duty cycle, and a higher duty cycle means that the signal is stronger. In terms of motor control, this means that the motor will move faster when the duty cycle is higher.

To configure a pin for PWM on the MCU, the datasheet must be referenced. On our selected MCU PWM signals are driven by a timer, so a pin with timer capabilities must be selected. This is represented with the "TA" attribute. This must be configured for reset/set mode which determines how the duty cycle is calculated. The value TA0CCR1 is divided by the value of TA0CCR0, where TA0CCR1 represents the amount of ticks completed after the timer resets to 0

and TA0CCR0 represents the amount of ticks in one clock cycle. The signal is “high” after the reset and is set to “low” after reaching the TA0CCR1 value, creating the pulse width modulation. With this, the TA0CCR1 value can be modified to control the motor as needed for the corresponding delay time.

With the DRV8825 motor driver, the maximum frequency that can be used to modulate is 250 KHz. The MCU used has a configured 1 MHz clock. The timer feature allows this clock frequency to be divided by 1, 2, 4, or 8 to slow the timer down. A divider of 8 was used to ensure that the frequency was 125 KHz, well below the maximum allowed for the driver. In practice, a duty rate of 1/32 was used to ensure micro stepping with a clock period of 1024 ticks. 1024 ticks / 125 KHz = 8.192 msec/tick, well above the minimum step time of 1.9 microseconds. This gave some leniency on the motor’s rotation as well as the ADC reading.

#### 7.1.3.2 Analog-to-Digital Converter Details

The ADC must be configured through a variety of different configuration settings. The primary setting to configure is the sample-and-hold time (SHT) which determines how long the ADC takes to settle the electrical value before converting it into a digital value. To calculate this, the formula $(RI + RE)*(CI + CE)*\ln(2^{N+1})$. RI and RE are the internal and external resistances while CI and CE are the internal and external capacitances. N is the bit resolution of the ADC, 10 in this case. In the MSP430’s datasheet RI = 1k and CI = 27 pF, and on the PCB RE = 11.7k and CE = 47 pF. The result came out to 7.1673 microseconds. To convert to the amount of clock cycles needed, multiply by the clock frequency which equal 1 MHz. This equals 7.1637 which rounds up to 8 clock cycles.

Also configured was the channel used for the ADC. This was found by checking the pinout of the PCB schematic, which had the connected pin with ADC channel 12.

#### 7.1.3.3 Synthesized Operation

To properly perform a sweep, the motor must be started and stopped many times, as well as changing directions to return to its original position. This is handled by using a second timer channel in “up mode”, in which it counts up to a specified value before stopping and raising a flag. To properly synchronize, the upper limit was set to 1024 ticks, the same as the period for PWM. This ensures that only 1 pulse is sent to the motor before being stopped, keeping precise movements and avoiding misalignment with the diffraction grating. A for loop was used, with an upper limit equal to the resolution of the sweep to be performed. This repeatedly sets the PWM duty value to 32, restarted the timer, then set to 0 upon completing one pulse. The ADC is then read, the 10-bit value split into 2 8-bit values, and both are sent to the PC over UART. After this loop completes, the motor’s direction is reversed through a GPIO pin being used for output. This value is switched and a new loop begins, simply starting and stopping the PWM, synchronized by a timer. This repeats the exact same amount of times as the first loop, ensuring that the same amount of steps are taken in both directions.

## 7.1.4 FREG PCB Software

The FREG PCB uses an ESP32 family MCU and is programmed using Arduino IDE. This makes code very simple to implement with high-level functions for many features. The LiquidCrystalI2C library is also used to display characters on the connected I2C LCD module on

the PCB. This includes functions to initialize, clear, and write to the LCD without needing to manually set I2C values. Before this can be used, an I2C scanner must be used with the LCD plugged in to acquire the correct I2C address of the device.

In the operation of the code, a serial connection is established with the computer with baud rate of 9600, and the LCD is initialized. The shapes which make up the bar are also defined in the setup, using columns of bits to create a moving bar. In the loop function, the code waits for activity on the serial port. The first value sent is read as the upper limit of the progress bar, which equals the resolution of the spectrogram. Future serial instructions fill the progress bar by using the write function, as well as updating the value in #/Res format (ex. Progress: 64/128).

## 7.2 PC (MATLAB) Software

The software on the computer connected to the FREG system must handle 3 key elements of the overall operation: assembly of the spectrogram, deconvolution of the spectrogram via the FREG algorithm, and display of the necessary data to the user. Each of these elements will be visually described with a software flowchart, then textually described in 3 subsections.

### 7.2.1 Software Flowchart

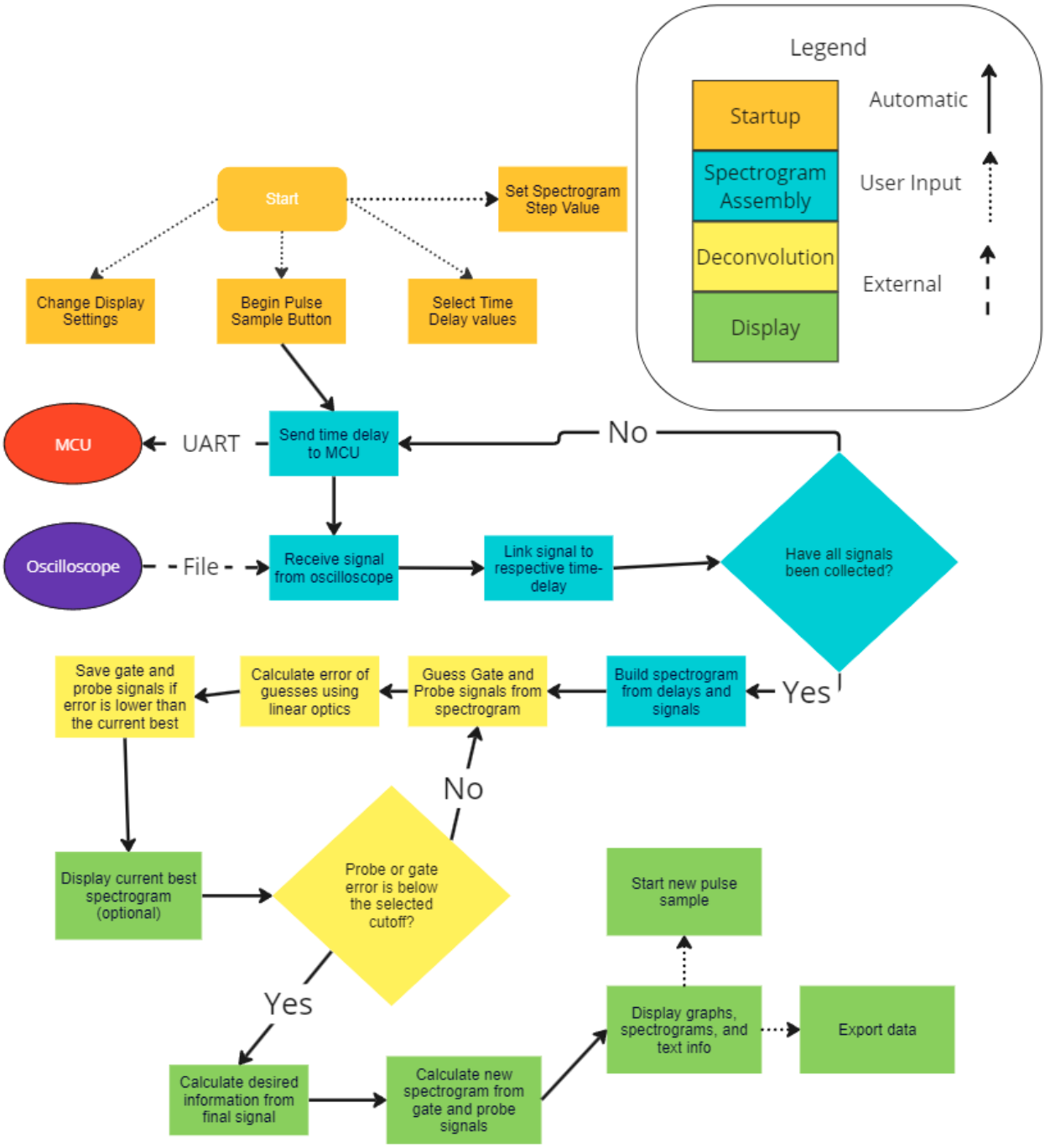



Figure 32: PC software flowchart showing the operation of the code

## 7.2.2 Spectrogram Assembly

### 7.2.2.1 Overview

To get the spectrogram of the laser pulse, the outputs of the OSA must be pieced together. This is done by associating the signal with its respective time delay produced by delay line. To do this, a matrix is created and filled. Each row represents the full spectrum of a the pulse at a given

time delay. The x-axis is the wavelength, determined by associating the motor rotation angle to the reading of the PD. The y-axis represents the increasing time delay applied to the pulse on one arm of the beam splitter.

#### 7.2.2.2 Initialization & Data Acquisition

To initialize the FREG, serial connections must first be established. In the full setup, there are three serial connections to establish: FREG, OSA, and TDL. After connecting to these, the resolution is selected, which is always a square and in increments of 16 (e.g. 64x64). To begin the acquisition, a MATLAB script is used within the app. It begins by properly formatting multiple values to send UART values to the TDL with hex-codes and sending the initial value to the FREG PCB for progress display. It then begins a loop with a number of steps equal to the resolution value. Within the loop, a UART value is sent first to the OSA PCB to perform a sweep. The data is acquired with 2 UART readings (top 2 bits + lower 8 bits) and then converted back to the true voltage, using the formula Vreal = 3.3 * (Vadc / 1023). These values are then stored in the first row of an empty matrix. Within that loop iteration, the FREG PCB recieves a progress update and the TDL receives its necessary time delay instruction. This repeats until the matrix is completely filled.

#### 7.2.2.3 File Management

The spectrogram matrx must then be placed in a file that can be understood by the Trebino deconvolution code. This is known as the .frg file type. It requires a first row that includes the resolution, spectral resolution, temporal resolution, and central wavelength. Afterwards, the FREG matrix data must be written, delimited by spaces and newlines on each row. To do this the first row is printed immediately before the matrix. Then, using another loop, each value of the matrix is printed into the file using the append permission to avoid overwriting data. This file can then be used for deconvolution.

## 7.2.3 FREG Algorithm

The FREG Algorithm takes in the spectrogram that was previously assembled and seeks to acquire the pulse phase and intensity of the laser. This is done by deconvolving the spectrogram using the Generalized Projections algorithm as selected in subsection 3.3.3. This uses a probe function P(t) and gate function G(t), which are the vectors that make up the outer product of the spectrogram. These are first guessed by using Gaussian vectors and are then tweaked until the outer product calculated is identical (or very similar depending on parameters) to the spectrogram input.

The key portion of code for the FREG algorithm is a loop which handles the adjustment of the gate and probe functions. The loop will run as long as allowed based on the selected settings: the gate and probe functions each have a designated cutoff point after which the loop will break. Lower cutoffs will give the algorithm more iterations to hone the functions, creating a more accurate result, while higher cutoffs will reduce the time it takes to run the code. In each iteration of the loop, nonlinear optics methods are used to calculate how similar the retrieved FREG spectrogram is to the input spectrogram, known as the error value. The error value is calculated, then the function is shifted to create a new guess. This is done for both the gate and probe functions. Depending on the selected parameters, the best gate or probe function is then compared to the new function, and if deemed more accurate (the error is lower than the current best), both the gate and

probe are updated as the new best generated functions. The current iteration of the functions are also displayed or printed based on the selected settings.

After the loop, the final versions of the input spectrogram, the retrieved spectrogram, and the calculated phase intensity graphs are displayed and/or printed, which is discussed further in the following User Interface subsection.

#### 7.2.3.1 FREG Helper Functions

To perform blind deconvolution, multiple helper functions are used to streamline the process. Some of these are included in MATLAB packages while others must be created specifically for use in the program.

##### 7.2.3.1.1 MATLAB Functions

Many math functions will be used in the deconvolution process which was the main reason for selecting MATLAB. A large number of these functions are within the signal processing toolbox, including the fast Fourier transform (fft) and inverse fast Fourier transform (ifft) functions. This is used to switch between time and frequency domain for a signal which has multiple uses, most directly to display the extracted phase intensity graph in both the time and frequency domains.

Calculus functions also play a major role in deconvolution. Differentiation for polynomials with the “polyder” function and calculating the roots of a function are necessary in determining the error of the gate and probe signals.

As discussed in subsection 7.1, the MCU on the PCB will communicate the delay values from the time-delay line to the PC. This is done using UART, which connects to a serial port on the computer. MATLAB has a function named “serialport” which allows the programmer to collect values from the serial port into MATLAB. The associated function “write” will be used to send the delay value to the time-delay line with help of the MCU to allow for the spectrogram to be assembled properly.

## 7.2.4 User Interface

Two user interfaces are implemented into the system: one for pulse acquisition and the other for deconvolution, known as the frogger.

#### 7.2.4.1 Pulse Acquisition UI

This UI was created in MATLAB app designer. It features fields for serial port connections and the spectrogram resolution, as well as a file name. It features a button to connect to the serial ports and provides errors if there are issues such as duplicate ports or already used ports. After connecting, the user can click another button to begin the pulse acquisition which performs the code described in section 7.2.2. Finally, it features buttons to access the optional binner for spectrogram cleanup, or directly to the frogger for deconvolution.

#### 7.2.4.2 Frogger UI

The frogger program, created by Georgia Tech’s ultrafast optics department, handles the deconvolution of the FREG pulse. It displays the real spectrogram as well as an updating recreation of that spectrogram which moves as the algorithm attempts to recreate it. The pulse amplitude and

phase graphs are also displayed, in time and frequency domains. The Z and G error values are displayed in both text form and on a graph to see how they increase or decrease. Finally, a difference image is displayed to show differences between the real and retrieved spectrograms.

#### 7.2.4.3 Custom Acquisition UI

Due to an issue with the time delay line used, a version of the code was also created without TDL communications. This is shown below.

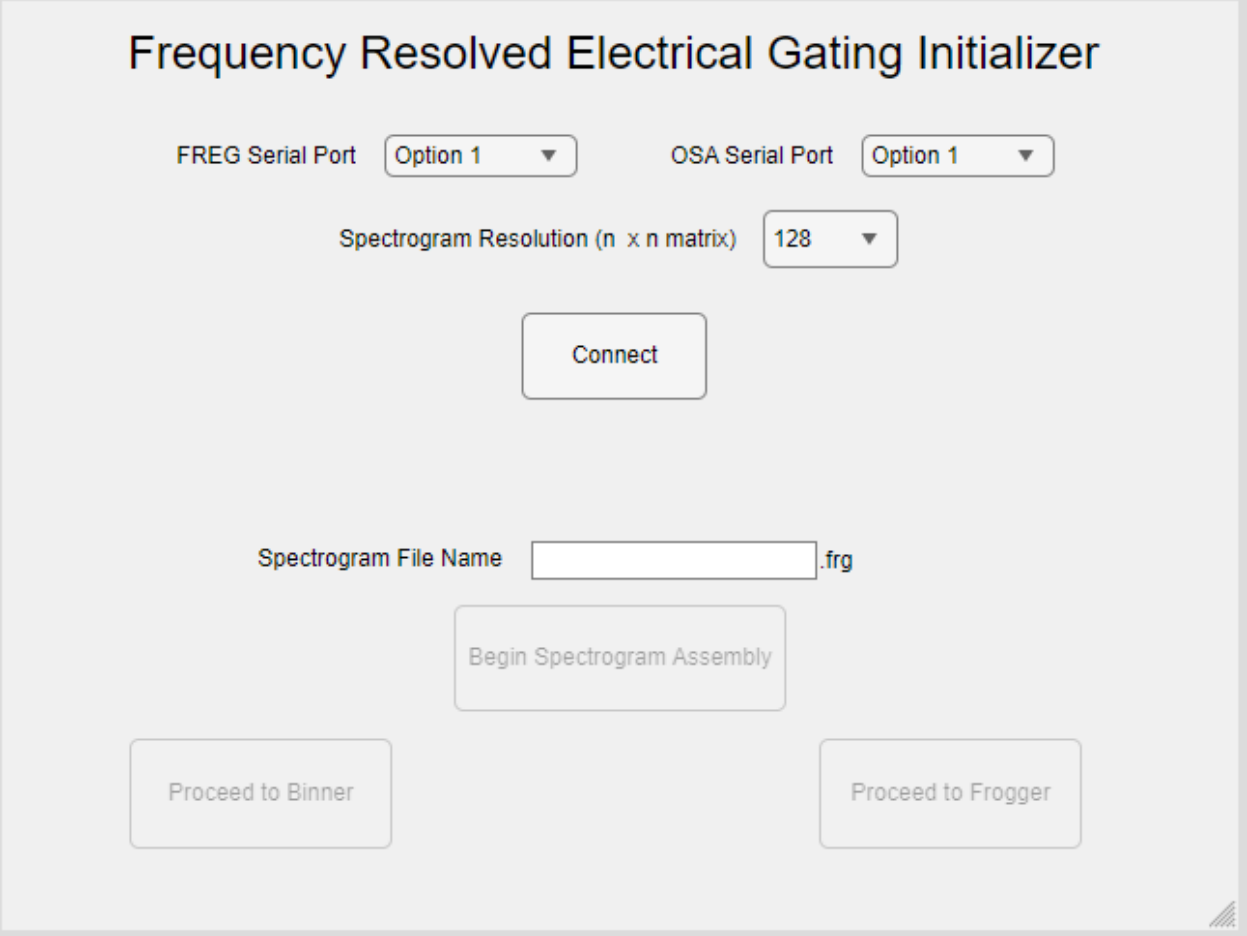



Figure 32: UI diagram for the pulse acquisition program

# Chapter 8 System Fabrication and Prototype Construction

## 8.1 PCB Layout

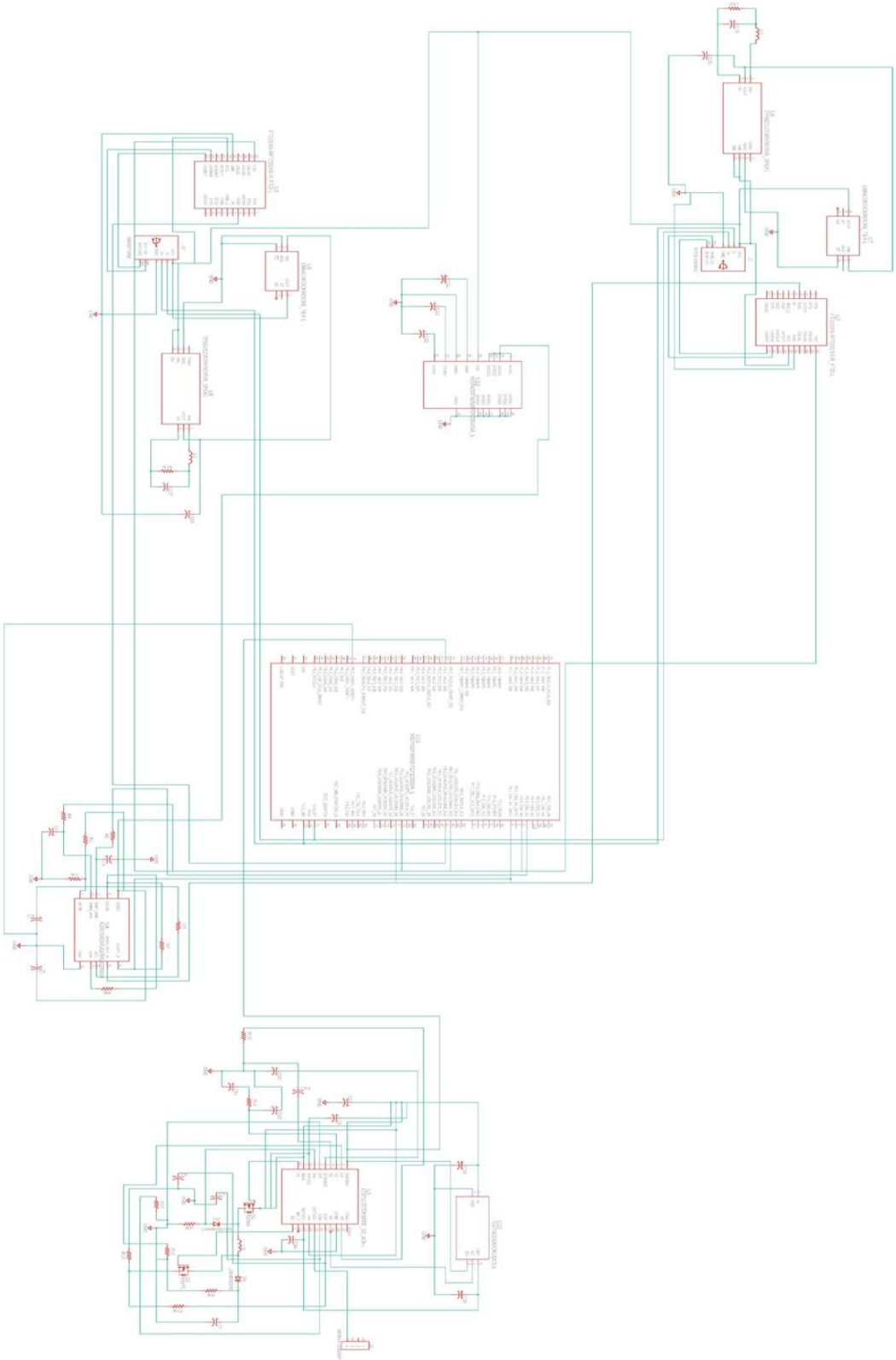


Figure 33: Overall PCB Layout.

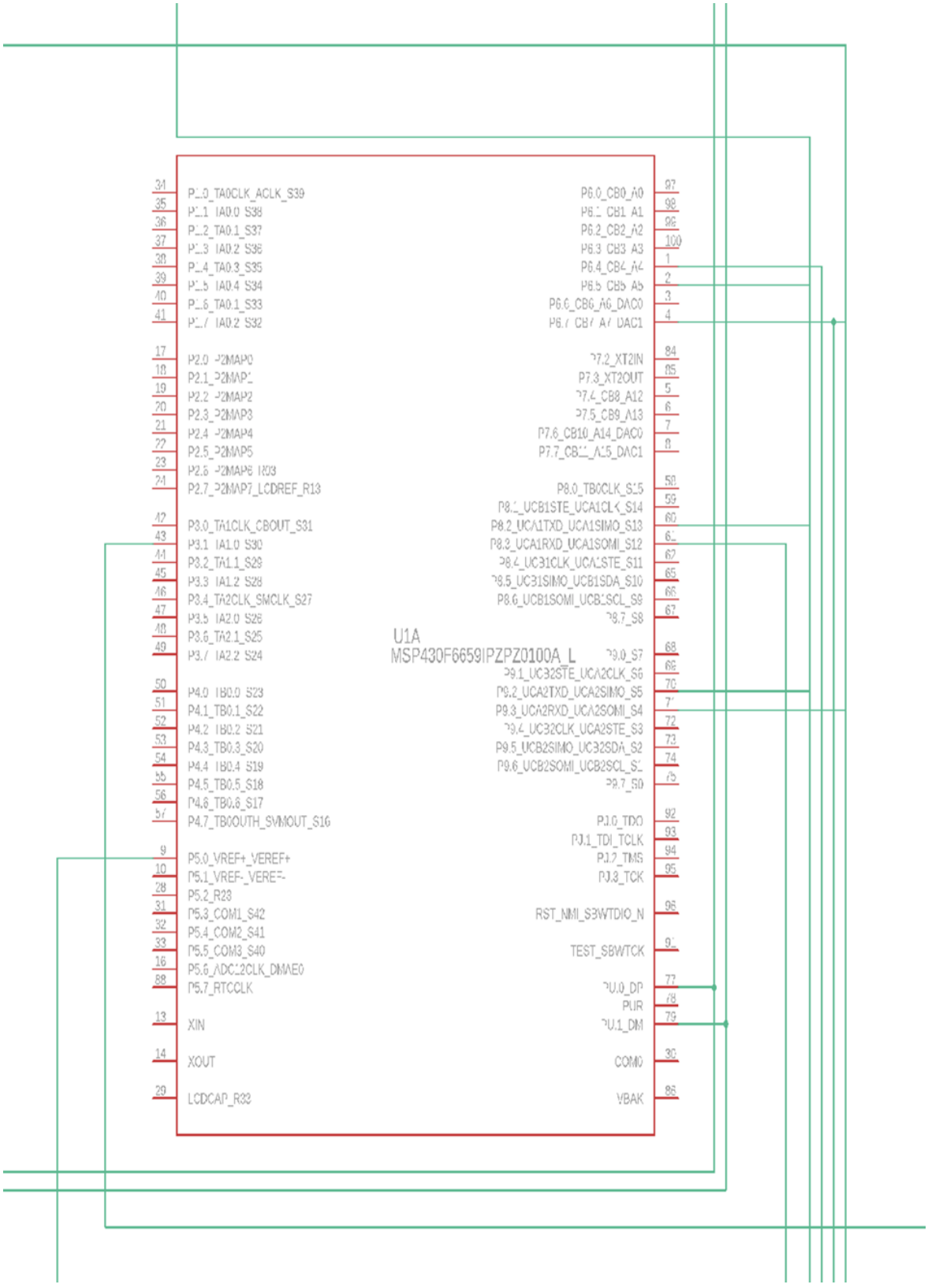


Figure 34: Microcontroller Connections

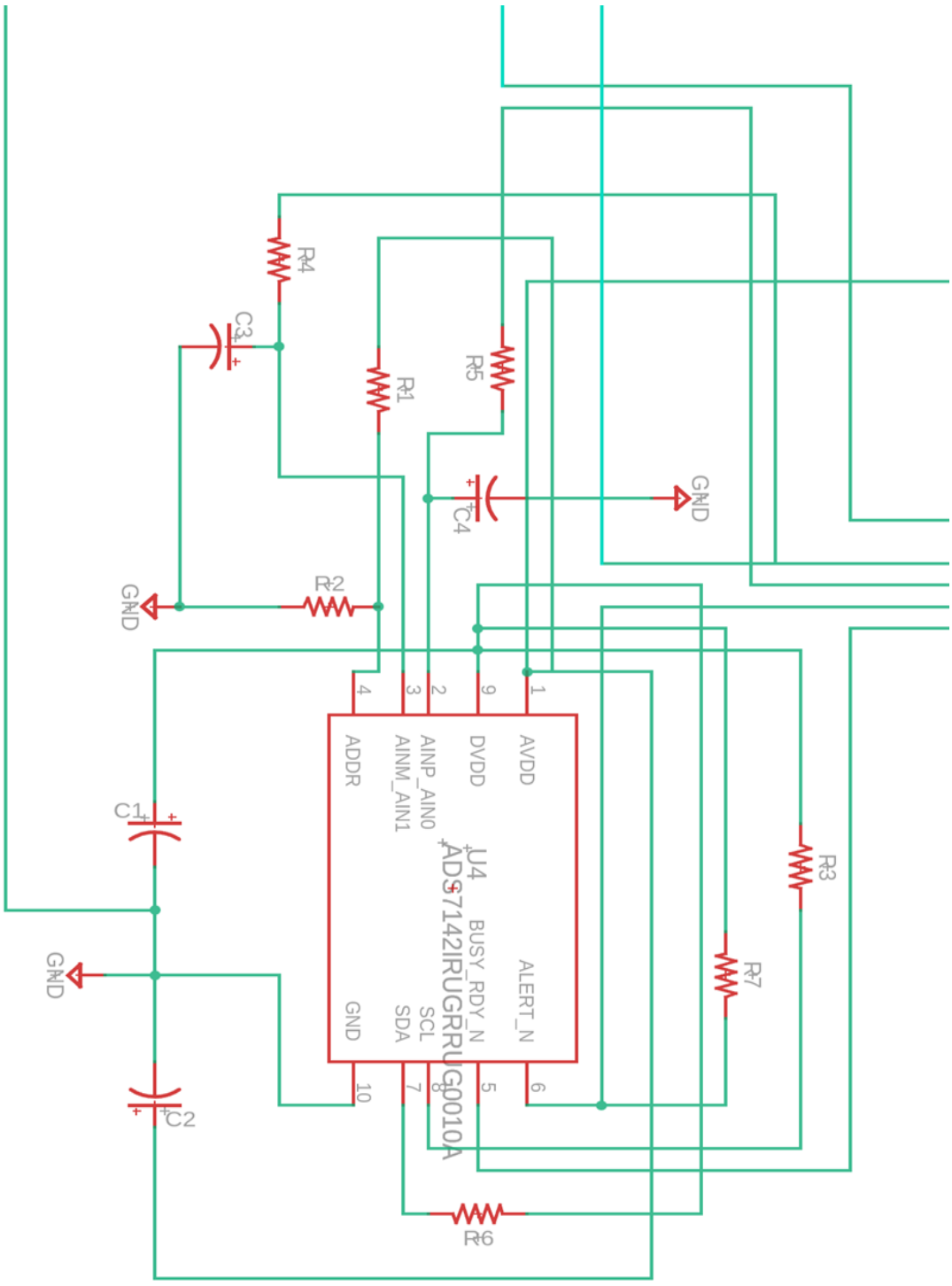



Figure 35: SAR ADC

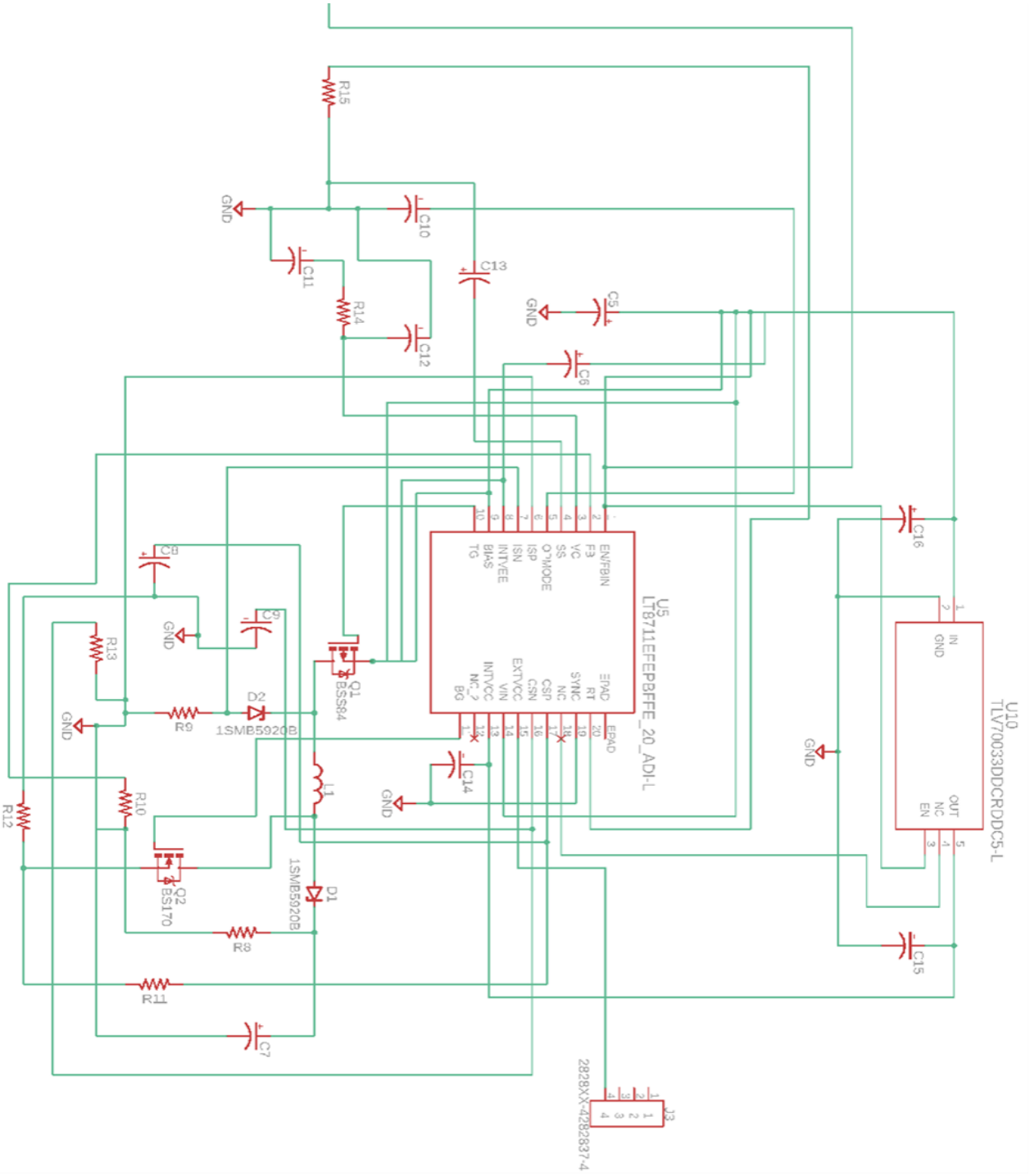

R15
GND
C10
C11
C13
R14
C12
C5
GND
C6
C16
C8
C3
GND
R13
GND
R9
D2
1SMB5920B
Q1
BSS84
U5
LT8711EFEPBFFE_20_ADI-L
EN/FBIN
F3
VC
SS
O*MODE
ISP
ISN
INTVEE
BIAS
TG
EPAD
RT
SYNC
NC
CSN
CSP
EXTVCC
VIN
INTVCC
NC_2
BG
U10
TLV70033DDCRDDC5-L
IN
GND
OUT
NC
EN
GND
C14
GND
L1
R12
R10
Q2
BS170
1SMB5920B
D1
R8
R11
C7
C15
2828XX-428283?-4
J3

Figure 36: PWM Controller

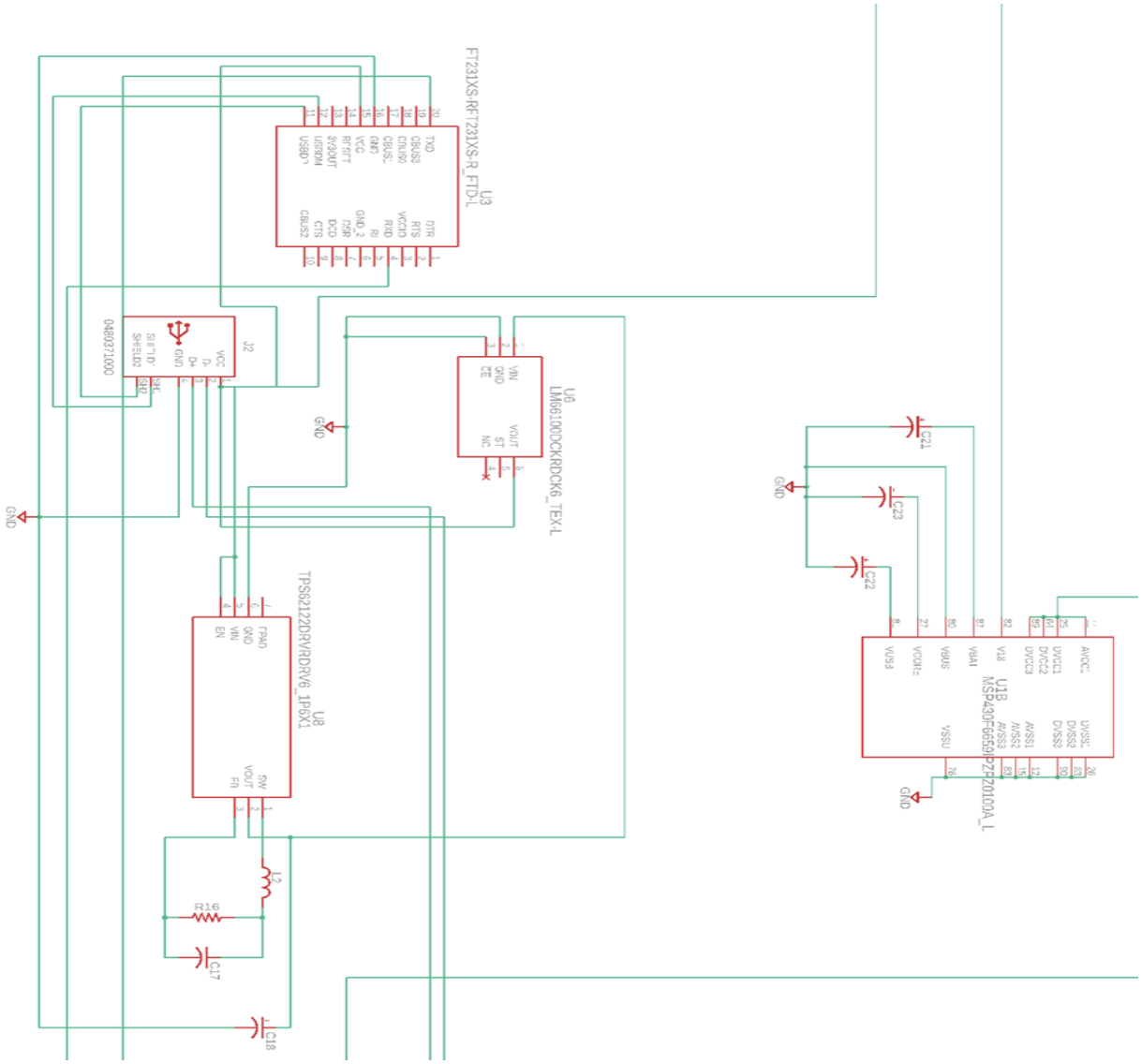



Figure 37: Time Delay Line USB-to-UART Bridge

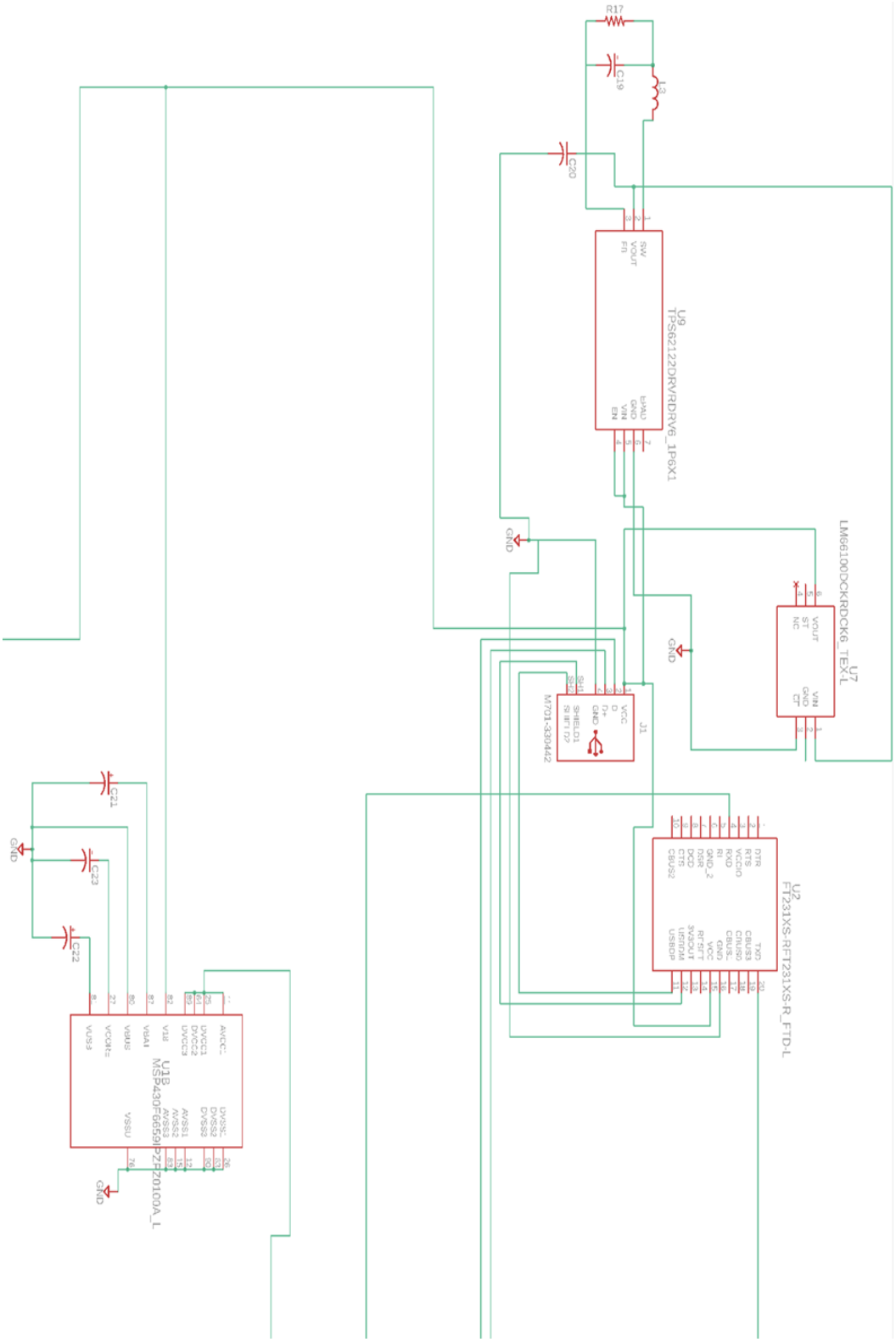



Figure 38: PC USB-to-UART Bridge

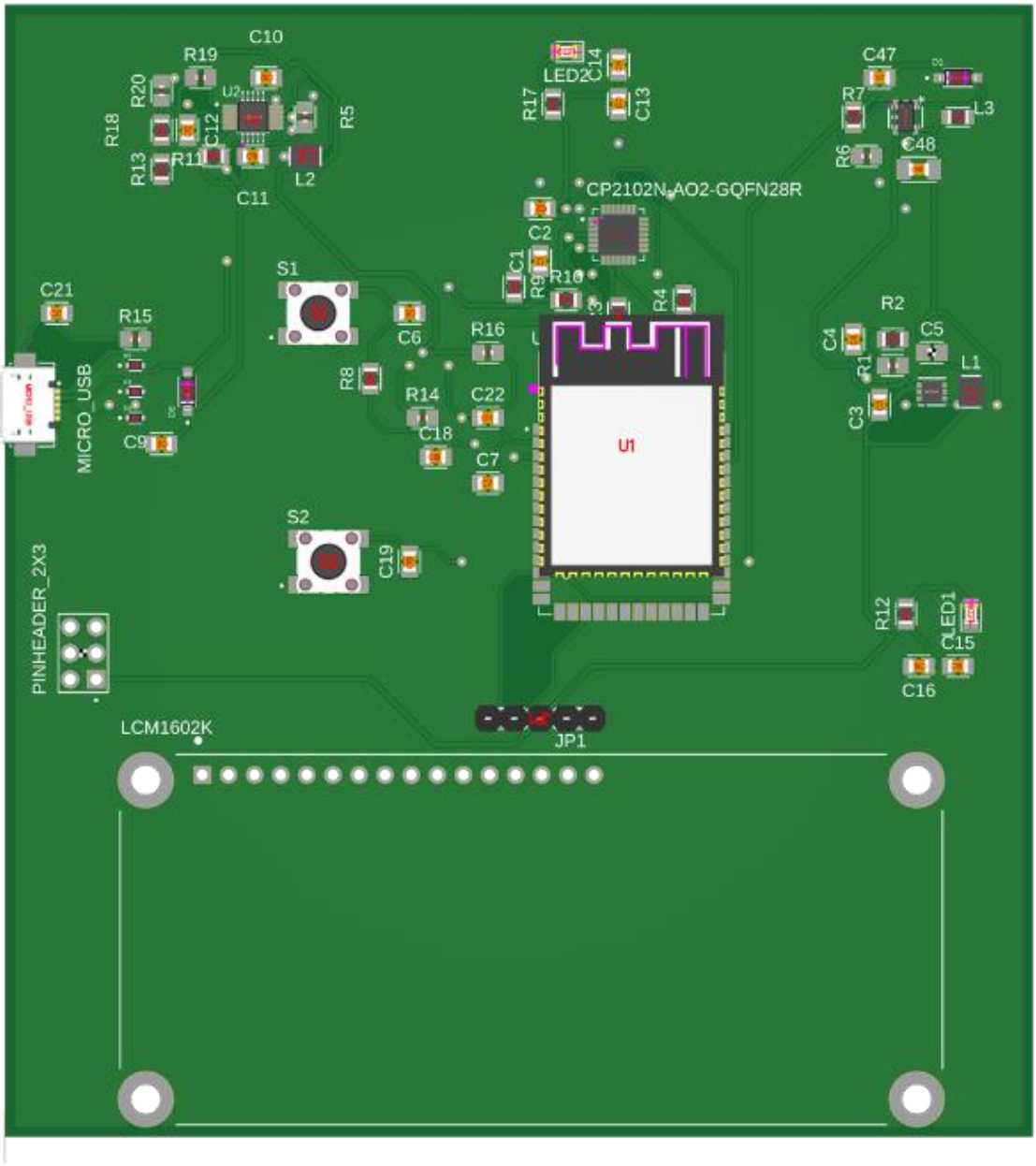



Figure 39: FREG PCB Layout Render

## 8.2 Housing

The housing structure of the system has to be created using a material that is able to handle high sensitivity for the FREG as well as manage proper weight distribution throughout the system. There are some components in the FREG that are larger in size such as the time delay line that has to be integrated in the layout, however the mass of the device is too large for a typical ABS filament from a 3D printer to handle. The platform could potentially be a metal tray or an optical breadboard, but the top cover and walls would be wooden planks. Once the FREG system is setup, then there will be a separate housing for the OSA. The sponsor is interested in utilizing the OSA for other setups, therefore it is in the best interest to keep the enclosures disconnected. Due to the

free space optics being performed in the OSA once the beam leaves the Mach Zender Modulator, the clear acrylic walls will not be ideal because there could be some causes of light reflections from the acrylic to the mirrors if the system was not aligned correctly. Instead of replacing the material however, we could create a shield to cover the clear lining where the beam paths go to prevent any light scattering or any reflection losses. This will keep the housing unit as light weight as possible along with maintaining cost efficient materials.

Another layout design for the housing enclosure is to make it a two-story enclosure. This setup is to make it more convenient by having the optical layout be both first and second level to keep it concise. The first layer will have the setup of the FREG on an optical breadboard while the second layer will have the most of the electrical components and the OSA portion. This idea was to ensure the setup has two separate areas that are easily accessible. By being able to attached and detach the system, this allows us to make any modifications to the system without having to recreate the whole system. The first layer is completely separate from the OSA therefore we are able to make any mechanical changes without it disrupting the second layer. The second layer flooring with the OSA will be made of wooden planks This will enable us to see the first and second layers interchangeably without having any obstruction of viewing. By having a small peep hole on the wooden stucture. The second layer will have to be mounted down, therefore there will not be a need for an optical breadboard layout. The only moving component will be the motor while the rest of the OSA is locked down by either screwing the components directly on the wooden board or clamping them down. The PCB and time delay line will be mounted on top of the first layer as well, but they will be sectioned off to not affect the OSA.

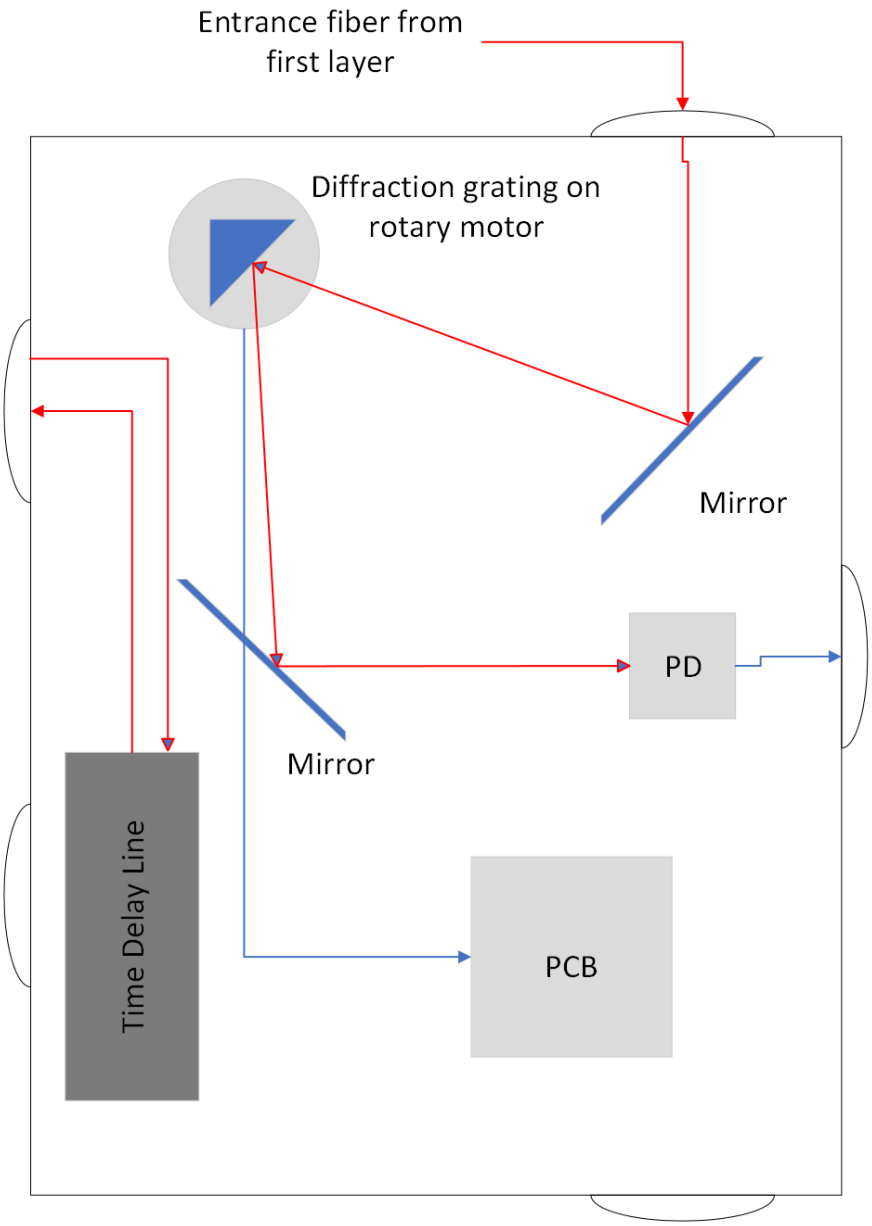



Figure 40: This is the Second layer of the enclosure that will hold the time delay line, OSA, and the electrical components.

As shown from Figure 40, this is the two-layer setup that will contain all of the components onto one optical breadboard. The second design incorporates the OSA and the FREG and housing the electrical components. For this reason, the second design will most likely be the final design for the entire system.

# Chapter 9 System Testing

## 9.1 Optical Hardware Testing

As far as the optical hardware, devices which require testing included the beamsplitter, the optical fiber splices, the polarization controller, the electro-optic modulator, the time delay line, photodetectors, the overall OSA design, and the FREG design.

The beamsplitter was testing was done by varying the amount of input power into the beam splitter and measuring the output power at each of the output arms. We assumed that the power ratio advertised on the beamsplitter was accurate (90-10), thus we assume any discrepancies measured were due to insertion, polarization-dependent, or return losses. Shown below in Figure 41 is the obtained data for the beamsplitter characterization.

| Max Laser Power | > 2 mW | | | | | |
|---|---|---|---|---|---|---|
| | | | | | | |
| Power Incident (W) | Blue Power (W) | Red Power (W) | Blue % | Red % | Sum % | Loss (dB) |
| 1.10E-03 | 9.59E-04 | 9.33E-05 | 87.18% | 8.48% | 95.66% | -0.19 |
| 1.00E-03 | 8.60E-04 | 8.34E-05 | 86.00% | 8.34% | 94.34% | -0.25 |
| 1.20E-03 | 1.05E-03 | 1.00E-04 | 87.58% | 8.37% | 95.95% | -0.18 |
| 1.30E-03 | 1.14E-03 | 1.09E-04 | 87.54% | 8.40% | 95.94% | -0.18 |
| 1.40E-03 | 1.22E-03 | 1.17E-04 | 86.79% | 8.37% | 95.16% | -0.22 |
| 1.50E-03 | 1.31E-03 | 1.27E-04 | 87.53% | 8.45% | 95.99% | -0.18 |
| | | | | | | |
| | | Average | 87.10% | 8.40% | 95.51% | -0.20 |

Figure 41: Shows the testing data done for characterizing the beamsplitter. The “Blue” refers to the arm which 90% of the power is split into, the “Red” refers to the arm where 10% of the power is split into.

Table 26: Comparison of the Beam-splitter actual losses to the expected losses.

| | 90% (Blue) Arm | 10% (Red) Arm |
|---|---|---|
| Insertion Loss (dB) Measured | 0.14 | 10.30 |
| Insertion Loss (dB) Expected | 0.53 | 10.57 |

Table 26 shows the final results, comparing the insertion loss between what we measured and what was expected for the beamsplitter. We completed this post-polarization optimization through the beamsplitter, thus we assumed that any excessive polarization-dependent losses are not added by the system. We find that the error between the expected values of the insertion losses and actual values to be 9.4% and 6.4% for the 90% and 10% arms respectively.

The optical fiber splices were characterized via the usage of an OTDR, or optical time domain reflectometer. This device sends a test signal into the system and measures the power reflected to the OTDR and tells us the origin location of those reflected signals. We can use this to

characterize major losses in our system due to fiber splices, or optical connections from one device to another which may not be stable.

The method by which we optimized the polarization controller of the system was by connecting the output of the unbiased electro-optic modulator to a power meter. We then adjusted the polarization controller until the output power was maximized. Because the system is not polarization dependent, we only need a polarization controller porting into the MZM, due to the polarization dependency of the Lithium Niobate. Optimizing the input polarization to the modulator is vital to increase the efficiency of the power transfer into the modulator. Otherwise, we are not concerned with the politization throughout the system.

Another test was done with a 50:50 beam splitter in order to have more optical power through the fast photodiode in the FREG system The diode that is in the FREG must have an optical power higher than 1 mW, which was not the case in the 90:10 where we are at 0.27 mW. This isn't sufficient power for the 14 GHz photodiode to properly provide a signal through the modulator. When doing the test, there was significant contrast with the pulse overlapping on the OSA, which was desired to see how much of the pulse overlapping was occurring in the system.

The electro-optic modulator is characterized via applying a variable voltage to the DC bias pin of the modulator, then measuring the output optical power. We then charted the power output per voltage input, which produces the modulator DC biasing curve shown below in Figure 42. We utilize this modulator biasing curve to determine the best voltage to bias the modulator with. As explained in Section 6.1, we need to bias the modulator to the lowest possible output power. This allows the proper gating of the input pulse train, because it configures the modulator in a way which it only produces an output optical signal if the pulses are overlapped.

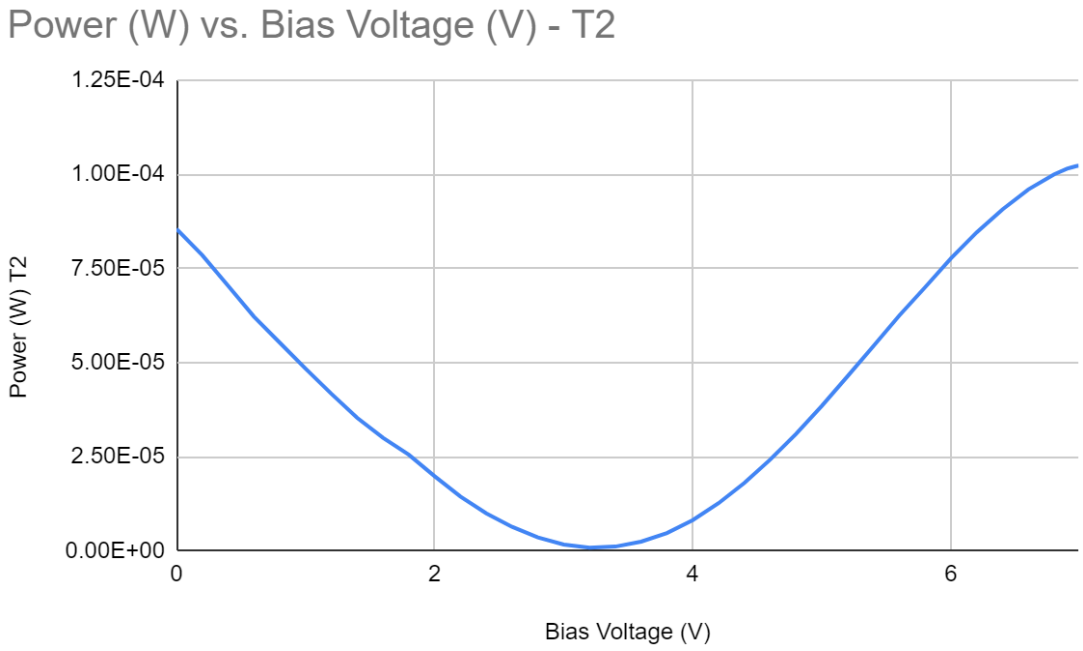


Figure 42: Shows an example of the modulator biasing curve obtained from testing. This was obtained for a JDSPhase 14 GHz MZM.

To test the time-delay line, we can utilize interferometry to determine whether the time-delay produced by the device is accurate. Specifically, we could use a method such as Michelson Interferometry to measure whether the time-delay is accurate. This would require us to measure the fringe shift produced by the interferometer to determine whether the phase difference between the optical signal produced by the time-delay line and the reference optical signal is accurate to what we would expect. We will need to test this at various time delays, for a span of approximately ±2 picoseconds.

For the photodetectors, we can simply input a known optical signal and use an oscilloscope to measure the output electrical signal. We can repeat this for different input optical powers, and then compare the output response to the spec sheet for the devices.

The portion of the OSA design that needs to be characterized is the relationship between the angle of the diffraction grating due to the motor and the band of wavelengths which are hitting the photodetector. We can characterize this relationship by using a known-wavelength source through the spectrum analyzer and measuring at which angle that wavelength hits the detector. Because we have a laser which is wavelength tunable, we can simply change the wavelength and repeat this measurement of the angle several times to find the relationship between the wavelength hitting the detector, and the angle of the diffraction grating. This relationship is not entirely linear, but for the small span of wavelengths we will be using in the FREG system, it can be approximated as such.

The FREG system testing will be similar to the OSA, because we will be using a known source, in terms of output wavelength, pulse energy, pulse duration, etc. to determine whether our system can accurately characterize the input optical pulse train from the fiber laser. We have two sources but will likely acquire a third to demonstrate the robustness of our system.

# 9.2 Electrical Hardware Testing

The In-Circuit Testing method will be implemented to verify the integrity of the soldering connections by placing probes at the access points on the board. A multimeter device will test for faults and the expected performance of all electrical components once the PCB has been fabricated. Utilizing the conductivity interface for the multimeter is necessary for determining if all routing and traces are functional by confirming the flow of current throughout the entire board. Additionally, the DC voltage setting is another option for conducting a sample test by connecting a low-power supply to the PCB to check for irregularities on the board before adding the time delay line or PC connections.

# 9.3 Software Testing

The software has 2 distinct parts to test: the MCU software and the computer software on MATLAB.

## 9.3.1 Embedded Software

To test the software on the MCU, the PCB can be isolated and connected to the PC and time-delay line. Code Composer Studio has testing methods such as a debug mode included in the software allowing for easy testing and tweaking of the code. The code will be flashed onto the MCU over USB and then run using debug mode which will immediately identify any errors or typos in the code.

To test the UART communication between the PC, MCU, and TDL, a terminal software such as TeraTerm can be used to monitor activity on the UART channel. Testing the link between the MCU and PC is simply tested by setting up a full-duplex UART connection and using code which has looping transmit functions with the reception from the direct PC keyboard input. If the MCU sends the same variable that is input by the PC, then the connection is successful. Testing the PC to TDL connection should be done after the PC to MCU testing. The delay line has an automatic system to transmit back the value that is sent to it which is beneficial in testing.

Testing the PWM setup to control the motor can be done by isolating the PC, PCB, and motor. Multiple different PWM duty cycles should be used to see what the resulting response is for the motor. This will allow us to determine what signals must be sent to the motor for the corresponding time-delays as well as ensuring that PWM is a viable method to control the motor.

The ADC software can be tested by applying a known value to the BNC connector on the board through a DC power supply. Reading the value and sending it over UART checks if the ADC reads anything. Then, the value can be converted to voltage to ensure that the right reading is being acquired.

The whole system is tested by combining all of the following tests and viewing the spectrum produced from a motor sweep on a program like MATLAB which can plot the array of values.

### 9.3.2 MATLAB Software

The MATLAB software can be tested without any hardware connections. Each section of the software can be tested individually to create a fully functional system without needing to manage a very large amount of code. The spectrogram assembly can be tested by creating sample signal functions with corresponding sample time delays. The result can then be displayed on a user interface and compared to a mathematically assembled spectrogram using those signals. If the spectrograms match, then the assembly code works properly.

Deconvolution in the FREG will be tested by using sample FREG traces. These can be created and used as an input for the code without the need for any optical hardware. This is done by convolving known gate and probe signals into a spectrogram, so we know the expected final signals of the algorithm. The spectrogram will then be run through the deconvolution algorithm within the code. To compare the results, the display code must be tested first which can easily be done by taking a spectrogram or any other image and running the display code using that as the input. The FREG algorithm’s retrieved FREG spectrogram and final gate and probe signals will be compared to the input spectrogram and signals. The closer the retrieved spectrogram is to the input, the more effective the FREG algorithm is.

Testing on real FREG traces requires the full setup to be complete. To produce spectrums without the OSA PCB, a commercial OSA can be used to acquire traces instead. A modification

to the FREG UI must be made to do so, and the values must be properly converted to power. Resulting traces can then be deconvolved using different settings and nonlinearities. Traces can also be “cleaned up” by removing extraneous data to assist in a smooth deconvolution.

### 9.3.3 MultisimLive Software

The MultisimLive software will be an integral part of simulating all the circuit designs for each component separately to verify that the system parameters are met using selected components. The simulations will provide feedback on which components are being supplied with the correct amount of current and voltage. Testing the USB connections from the time delay line can be simulated to see how it will affect various connections on the board. All calculations regarding values provided in the datasheet for all components can be checked in a live simulation which will give a full analysis of what the expected output values for various connection points on the board should be.

## 9.4 Results from Senior Design 2

For the optics portion of this project, the main objectives which were accomplished include the completion of the design, ordering of components, and characterization and building of the set-up. The spectrum analyzer will require further optimization of the design to improve the spectral resolution of the device. Then, we built a protype of the spectrum analyzer using components we already have in the lab. We then purchased specific components for our unique spectrum analyzer to make a spectrum analyzer which can be used solely for our system. These devices which need to be ordered include the diffraction grating, the motor, the mirrors, the photodetector, and the fiber.

Then, for the FREG system, we do not require any further design. We moved onto characterization of our FREG components, ordering, and assembly of the system. The FREG components which still need to be ordered include the MZM and the photodiode for another iteration of the FREG. Otherwise, we have the beamsplitter, time-delay line, and fiber, which can all be characterized via the methods enumerated in Section 9.1. Once this is completed for the components we have and the components we need to order, we can finally move onto building the FREG. We already have the components necessary to build a lower-bandwidth version of the FREG for the purposes of a proof-of-concept. Once we were able to achieve the desired functionality, especially with regards to pulse overlapping and a high-resolution spectrogram, we can move onto building the full-spec FREG system.

The software design plan for Senior Design 2 is fairly clear cut. The MCU code can begin development by researching through laboratory code from the embedded systems class. Pins can be configured, and registers set based on the datasheet and family user’s guide of the microcontroller. The basics of UART and PWM can also be experimented with by using an MCU LaunchPad to configure them, although the pins will be different. Once the PCB is assembled, the code can then be flashed onto the MCU and properly tested using the components. This part relies more on the arrival of components than the connected computer’s program.

The PC software can be designed without the arrival of hardware components. The computer engineering and photonics students can work together to dig through the Trebino FROG code to learn more about its operation. With the assistance of advisors, this code can be modified by removing any nonlinear optics elements which would be incompatible with the operation of the

FREG. The spectrogram assembly element of the software can also be created with MATLAB documentation and tested with sample pulses. These can then be run in tandem to test the full software by using sample FREG spectrograms. This trial and error will allow the system to be developed for maximum efficiency and ease of use.

# Chapter 10 Administration

## 10.1 Budget Estimates

Table 27: Budget Estimates

| Sub-System | Component3 | Price (Estimate) |
|---|---|---|
| FREG | Electro-Optic Modulator | $900.00 |
| FREG | Time-Delay Line | $2,230.00 |
| FREG | Fast Photodiode | $5,000.00 |
| FREG | Beam Splitter | $316.00 |
| FREG | Single Mode Fiber | $100.00 |
| FREG | Polarization Controller | $300.00 |
| Source | Mode-Locked Laser | $0.00 |
| OSA | Diffraction Grating | $130.00 |
| OSA | Motor | $23.00 |
| OSA | Photodetector | $310.00 |
| PCB | MCU | $18.23 |
| PCB | Interface Controller | $6.55 |
| PCB | USB-To-UART Interface (2) | $4.68 |
| PCB | PCB – Manufacturing and Assembly | $100.00 |
| PCB | Voltage Regulator | $0.40 |
| PCB | Switching Voltage Regulator | $0.44 |
| PCB | Power O-Ring | $3.00 |
| PCB | External SAR ADC Selection | $3.00 |
| PCB | PWM Controller | $8.00 |
| Total | | $9,453.30 |

## 10.2 Milestones

| **Senior Design 1** | Worker | Start Date | End Date | Days to Complete | % Complete |
|---|---|---|---|---|---|
| Divide and Conquer (10 pg) | Team | 9/1/23 | 9/14/23 | 13 | 100% |
| Research OSA | Team | 9/1/23 | 9/21/23 | 20 | 80% |
| Gather BOM | Team | 9/10/23 | 9/14/23 | 4 | 90% |
| Order components | K & N | 9/17/23 | 9/17/23 | 0 | 80% |
| D&C Committee Meeting | Team | 9/21/23 | 9/21/23 | 0 | 100% |
| Midterm Demo | K&N | 9/22/23 | 10/12/23 | 20 | 100% |
| 60 Page Draft | Team | 10/10/23 | 11/3/23 | 23 | 100% |
| 60 Page Committee Meeting | Team | 11/7/23 | 11/7/23 | 0 | 100% |
| Final Demo | Team | 11/6/23 | 11/30/23 | 24 | 100% |
| 120 Page Final Document | Team | 9/1/23 | 12/5/23 | 95 | 100% |
| Upload Demo Video | Team | 11/27/23 | 12/5/23 | 8 | 100% |
| Senior Design 2 | | | | | |
| PCB Assembly | O&A | 10/1/23 | 2/5/24 | 124 | 100% |
| Deconvolution Algorithm Implemented | Team | - | 01/29/24 | | 100% |
| Parts Ordering | Team | 10/1/23 | 12/22/23 | 82 | 100% |
| Critical Design Demo | K&N | - | 02/26/23 | - | 100% |
| FREG Prototype Built | K&N | - | 01/15/23 | - | 100% |
| OSA Prototype Built | K&N | - | 01/01/24 | - | 100% |
| Full-Spec FREG Built | | - | 02/15/24 | - | 100% |
| Full-Spec OSA Built | K&N | - | 02/15/24 | - | 100% |
| Test Full System | Team | 03/01/24 | 04/18/24 | - | 100% |
| Final Presentation | Team | TBA | | - | 100% |

Figure 43: Milestones Chart

# 10.3 Work Distribution

Table 28 shows the planned and completed distribution of work for the paper and the construction of the FREG.

| Table 28: Work Distribution | | |
|---|---|---|
| Required Work | Primary Contributor | Secondary Contributor |
| Optical spectrum analyzer design | Namisha | Keana |
| Software design – MCU | Alex | Odane |
| Software design – program | Alex | Namisha |
| Housing design & manufacturing | Keana | Odane |
| PCB development | Odane | Namisha |
| FREG design | Keana | Namisha |

## 10.4 LLM Declaration

We hereby declare that we have not copied any pages from the Large Language Model (LLM). We have not utilized LLM for drafting, outlining, comparing, summarizing, or proofreading purposes.

# Chapter 11 Conclusion

To conclude, the FREG system is a device for characterizing the phase and pulse amplitude of short, low energy laser pulse trains. This is done by combining optical elements with an electro-optic modulator and other electrical components, all driven by software on the PCB and with a connected computer. The measured pulses are of such a short duration that they cannot be measured with traditional methods such as the FROG. No commercial FREG devices exist, making the importance of the project clear. The research performed is summarized in this section.

The optical portion of this system was split into the FREG and the spectrum analyzer. In the FREG, we designed several aspects of the functionality. We began with the beam-splitter power ratio, as we needed to verify whether a 90-10 beam splitter would provide a sufficient bias to the modulator and enough optical output to produce a high-contrast, and thus high-resolution spectrogram. From the testing, we discovered that the 50:50 was the need ratio to provide adequate power through the fast photodiode. We then designed the fiber lengths to minimize dispersion, specifically we calculated what length of fiber dispersion would begin occurring for. We found this value to be larger than the scale of our system, however we will still limit the amount of fiber used to connectorize our system. Additionally, we discussed design parameters of a FREG spectrographic technique, specifically the requirements which need to be met in order to accurately and reliably retrieve the pulse information.

Moving onto the spectrum analyzer, we discussed various types of spectrum analyzers, each of the individual component selections, and the subsequent design and simulation. The spectrometer that was designed is a Czerny-Turner spectrometer which operates from 1515 – 1585 nm, with a 0.5 nm spectral resolution. Further optimization of this design will be necessary, before implementing it into the system. This is because the desired spectral resolution has not been met yet. This spectrometer will allow us to record the spectrum of the gated optical pulse trains outputted from the FREG.

The software used to operate the FREG was split into two parts: the software for the microcontroller which is within the FREG's housing and the software for deconvolution and display which is on a computer connected to the FREG via USB. The microcontroller software's main directive is to act as a communication bridge between three components essential for the FREG operation: the time-delay line, the OSA motor, and the connected computer. The PC software has the important tasks of assembling the time-delayed signals into a spectrogram, deconvolving that spectrogram to acquire the phase and pulse amplitude of the laser input, and displaying those results to the user.

In researching the best technologies to use the microcontroller to communicate between these components, UART was quickly found as the best protocol to use. This is due to the long physical distance between the delay line, PC, and the MCU, as all of them are connected through USB cables. The selected time-delay line also uses UART through USB by default, meaning that using UART was the simplest choice. To control the motor, PWM was the clear choice as controlling motors is one of its most common uses. Designing software using these technologies will be done by using the appropriate IDE for the microcontroller, in this case Code Composer Studio from Texas Instruments. The family user's guide and the datasheet for the MCU will be used to identify which pins should be configured for UART and PWM as well as the registers that must be set to transmit data properly.

For the computer software, a numerically oriented programming language was decided upon due to the intense mathematics needed to deconvolve a spectrogram. MATLAB was selected as the language mainly because an openly available FROG code is written in MATLAB, which can be used as helpful reference code for the FREG deconvolution. This uses the principal components generalized projections method to perform 2D blind deconvolution, which was also selected as the deconvolution algorithm for the FREG. The code will be developed with a user interface which allows the user to set the time delays, initiate the pulse sampling process by sending a UART signal to the MCU, and view the results of the process.

The FREG system power requirements consist of a multilayer PCB integration which will act as a communication link between the grating motor from the OSA, time delay line and PC. Two USB-to UART bridge implementations were added to the board design to allow adequate serial communication for the delay line and the computer. The PC will be connected via USB-to-USB Type B connection that sends instructions to the microcontroller executed by a MATLAB code. The time delay line connection is composed of a USB-to-UART integrations that transmits and receives data from the MCU which then instructs the grating motor in the OSA to perform precision rotations. The connection to the servo motor consists of utilizing a PWM controller that enables a signal to be sent to the motor allowing it to perform the instruction set communicated by the MCU. Voltage regulators, diode, capacitors, and other design components are present on the board to aid in maintaining the integrity of each individual circuit design contained on the PCB. Due to the design parameters of the system a multilayer PCB implementation was necessary to meet all the FREG system requirements.

The top layer will contain the electrical components and routing of traces between them. The bottom layer will be the reference plane containing the grounding topology for the components. This design choices allows for more flexibility in positioning all associated high-speed components in the same area with compromising on impedance balance on the board. RF development can be avoided with the integration of various techniques that are incorporated on the

board such as shielding, decoupling and the addition of a power ORing to mitigate various power supply by acting as a switch resulting in the reductions of faults and overheating of traces. A reset button along with LEDs and switches and other peripherals will be added throughout the PCB where necessary to complement numerous circuit designs sections. All design techniques including in the PCB were selected to optimize the performance of the board while maintaining low power dissipation and consumption preventing build up RF energy ensuring a low impedance board is sustained within the performance specifications of the FREG system.

There were several challenges throughout the project that had to be tackled in order to move forward in terms of progress. One of the challenges was the optical time delay line not being able to be implemented with the PCB because of the software that is embedded into the device. It can only be run through Windows or Linux instead of a PCB through supported drivers, therefore we couldn't use this strategy to time the motor to the time delay line. The USB device required a USB host, and both being a host and device was difficult for an MCU. The USB-to-UART chip within the TDL has no supported drivers for embedded systems. Another challenge on the software setting was file formatting, and the FREG files were shown to be difficult in organizing.

On the optical side of challenges, one of the difficulties was a large portion of the system being relied on the polarization state. This had to be optimized before every run as well as the bias to the modulator being adjusted and optimized before a sweep test could be taken. Due to the low optical power, the electrical signal could not be amplified to the desired power, however if we were to increase the optical power then the photodiode will risk being saturated. The TDL broke towards the end of the project, and we had to manually control the stepper motor in the device using a motor driver, making it no longer automated through the computer. Finally with the gate size taking up the entirety of the time delay range, it was difficult to retrieve a functional spectrogram. The way to resolve this issue is to use a faster photodiode with a lower driving voltage modulator, which we were unable to acquire in time for the final showcase.

In this paper, we have described the full design of a fully integrated FREG system. This system will be independent, as we have outlined the optical design of the FREG itself, as well as the spectrum analyzer needed to produce spectrograms, the deconvolution algorithm needed to retrieve the pulse amplitude and phase, and the PCB integration which handles communication between the different devices and automates much of the system. This system is useful for the characterization of unknown optical pulse train inputs from a device-under-test, whether that be from soliton fiber lasers, or photonic-crystal waveguides. We reinstate the importance of characterizing an optical pulse train's amplitude and phase for the purposes of knowing the pulse width and dispersion of these optical signals as they propagate through expansive systems. One important reason to build this system is that there are no commercially available alternatives. Another important quality of this system is that characterizing low-energy, ultrashort optical pulses in a way that is modifiable and relatively cheap is important, especially in research settings.

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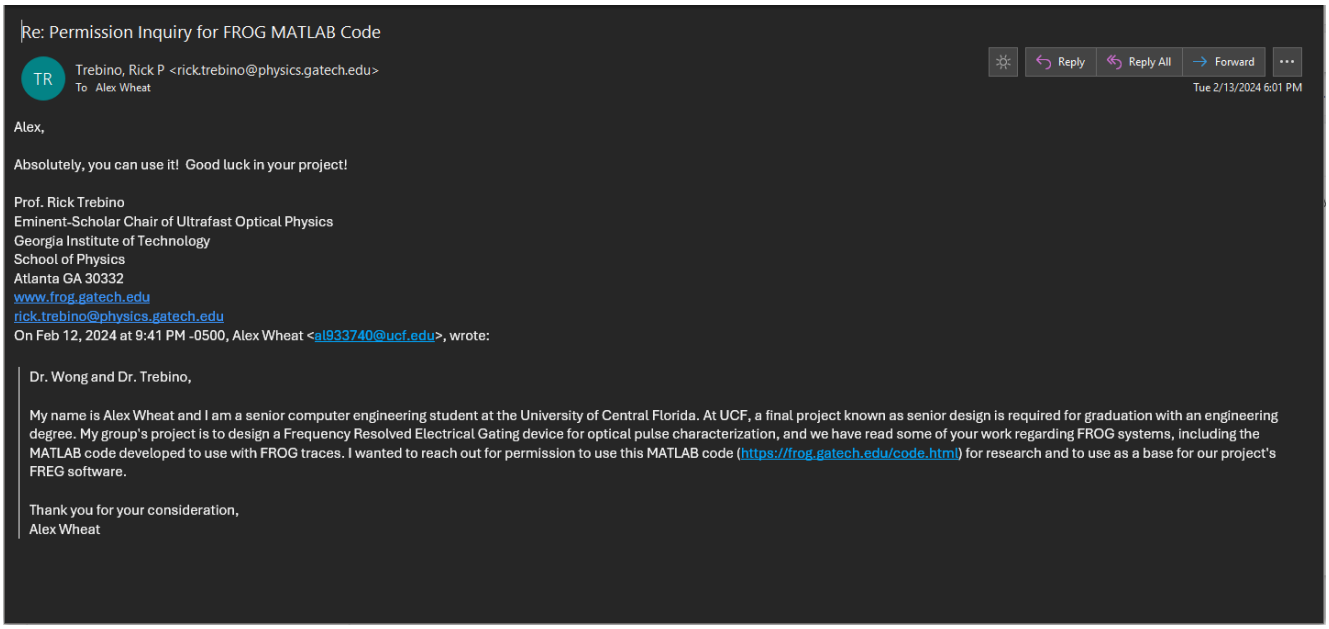
# Appendix B: Copyright

Permission to use the Trebino FROG code for this project:



Re: Permission Inquiry for FROG MATLAB Code

TR Trebino, Rick P <rick.trebino@physics.gatech.edu>
To Alex Wheat

Reply | Reply All | Forward | ...
Tue 2/13/2024 6:01 PM

Alex,

Absolutely, you can use it! Good luck in your project!

Prof. Rick Trebino
Eminent-Scholar Chair of Ultrafast Optical Physics
Georgia Institute of Technology
School of Physics
Atlanta GA 30332
www.frog.gatech.edu
rick.trebino@physics.gatech.edu
On Feb 12, 2024 at 9:41 PM -0500, Alex Wheat <al933740@ucf.edu>, wrote:

> Dr. Wong and Dr. Trebino,
>
> My name is Alex Wheat and I am a senior computer engineering student at the University of Central Florida. At UCF, a final project known as senior design is required for graduation with an engineering degree. My group's project is to design a Frequency Resolved Electrical Gating device for optical pulse characterization, and we have read some of your work regarding FROG systems, including the MATLAB code developed to use with FROG traces. I wanted to reach out for permission to use this MATLAB code (https://frog.gatech.edu/code.html) for research and to use as a base for our project's FREG software.
>
> Thank you for your consideration,
> Alex Wheat