Silicon optical nanocrystal memory

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We describe the operation of a silicon optical nanocrystal memory device. The programmed logic state of the device is read optically by the detection of high or low photoluminescence intensity. The suppression of excitonic photoluminescence is attributed to the onset of fast nonradiative Auger recombination in the presence of an excess charge carrier. The device can be programmed and erased electrically via charge injection and optically via internal photoemission. Photoluminescence suppression of up to 80% is demonstrated with data retention times of up to several minutes at room temperature. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1795364]

Silicon nanocrystal based nonvolatile memory devices[1] are now in advanced development and are expected to enter commercial production in the near future.[2] In these all-electrical memory devices, the conventional polysilicon floating gate is replaced by a dense array of silicon nanocrystals embedded in the gate oxide. Performance benefits expected from this change in the floating gate structure include improved retention times and improved radiation hardness due to decreased sensitivity to localized oxide leakage paths as well as improved prospects for CMOS integration due to reduced device aspect ratios. As we describe in this letter, a silicon nanocrystal floating gate additionally allows for the design of optically addressed memory devices that take advantage of the luminescence emission characteristics of silicon quantum dots[3–8] for data storage and retrieval.

Optical memory is a technology that could potentially replace electrical data buffers in optical communication systems and allow for the elimination of the accompanying optical-to-electrical conversion hardware. Previously, optical memory devices have been implemented in III–V quantum dot systems,[9,10] albeit at cryogenic temperatures. Room temperature operation is not possible in these devices because carriers are confined in relatively shallow potential wells. While similar devices have been fabricated in II–VI materials that can operate at room temperature,[11] silicon based optical nanocrystal memory offers the possibility for implementation in industry compatible fabrication processes.

The memory devices are read optically by monitoring the photoluminescence (PL) intensity, which varies according to the average charge state of the nanocrystals embedded in the device. The suppression of PL in charged nanocrystals is ascribed to fast nonradiative Auger recombination processes in which relaxation of optically generated excitons occurs by energy transfer to a nearby excess charge carrier.[12] Previous observations of PL "blinking" in isolated CdSe nanocrystals[13] and experiments in chemical systems in which excess charge is stored on II–VI nanocrystals via a change in solvent pH[14] confirm that PL can be suppressed in this way. Auger recombination is frequently considered to be an undesirable and potentially performance limiting process in nano-

crystal optoelectronics, but we exploit Auger processes in these devices to actively modulate the PL output.

We demonstrate optical erasure of the charge state of nanocrystals in the floating gate via internal photoemission after an electrical write operation. This erasure process is analogous to the procedure used in UVEPROM technology. We have observed evidence of optically assisted electrical hole charging of nanocrystals. Purely optical charging of nanocrystals may be possible in addition to optical discharging, but will require further designs.

The silicon optical nanocrystal memory devices designed for this study are single reticle ring gate transistors with optically transparent gate electrodes fabricated on 300 mm p-type silicon wafers. An initially grown 15 nm dry thermal oxide was implanted with $^{28}Si^+$ ions producing a distribution of silicon rich oxide with a peak composition of $Si_{1.75}O_2$ at a depth of $\sim$10 nm as calculated with the TRIM Monte Carlo simulation code.[15] The wafers were then annealed in a rapid thermal annealing furnace above 1000 °C in an atmosphere containing 2% O_2 by partial pressure to precipitate nanocrystals from the supersaturated solid solution. The background oxygen pressure is utilized to suppress changes in the stoichiometry of the gate that may result from preferential oxygen desorption during the annealing process.[16] A 40 nm polysilicon layer was then deposited to form a semitransparent, conducting gate contact layer. Subsequent photoresist patterning and etching was used to form ring gate transistor and MOS capacitor structures. Blanket implantations of $^{15}P^+$ and $^{33}As^+$ were used to degenerately dope both the gate contact and the source drain regions. A cross-sectional sketch of the device structure appears as an inset in Fig. 1.

Transmission electron microscopy in cross section was used to confirm the dimensions of the gate stack. Individual nanocrystals could not be resolved in these images due to low contrast between silicon and SiO_2. The presence of Si nanocrystals in the oxide layer was independently verified using vacuum scanning tunneling microscopy measurements on samples in which the oxide layer of the gate stack was partially removed with buffered HF.[17] From these measurements, we determine that the areal density of nanocrystals forming the floating gate array is at least $\sim$4$\times$10^{12}/cm^2 and

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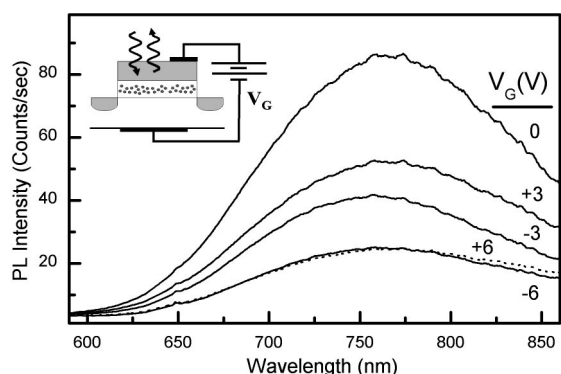   2622   © 2004 American Institute of Physics

FIG. 1. Steady state PL spectra measured under various applied gate biases. Inset shows a schematic of the device indicating optical addressing of the nanocrystal floating gate through the semitransparent gate contact.

FIG. 2. Capacitance $(C-V)$ and photoluminescence (PL) hysteresis loops (a),(b) measured at the same voltage sweep rate (50 mV/s) demonstrate data retention in this device. PL quenching is attributed to nonradiative Auger recombination in charged nanocrystals. PL decay lifetimes recorded at various gate biases (c) suggest that uncharged nanocrystals are also indirectly quenched by exciton migration to charged nanocrystals.

that the nanocrystals are $\sim 2-4$ nm in diameter. A maximum bound on the areal density can be derived from the total fluence of implanted silicon ions and is estimated to be within an order of magnitude of our lower bound. The discrepancy between these bounds may indicate a loss of nanocrystals during the partial etching procedure, a large population of small diameter (<1 nm) nanocrystals, and/or a significant loss of material to the bulk during the high temperature nanocrystal formation anneal.[18]

Device fields cleaved from the wafer were patterned with electrical contact pads consisting of a 10 nm Cr wetting layer followed by 100 nm of Au using a thermal evaporation and liftoff process and subsequently mounted in a Au wire bonded 40 pin ceramic dual inline package. The packaged devices were optically addressed in free space using an Ar$^+$ pump beam at 457.9 nm focused to 1 mm^2 spot and simultaneously electrically addressed. A cryogenically cooled CCD array and a grating spectrometer were used to collect PL spectra. All spectra were corrected for detector sensitivity. Stray light was removed by optical filters. PL lifetime traces were collected with a thermoelectrically cooled photomultiplier tube and a grating spectrometer under excitation by an Ar$^+$ laser modulated by an acousto-optic modulator.

Figure 1 shows PL spectra of a device in the uncharged state and also in steady state under various applied gate biases. The spectra peak near 760 nm with a FWHM of 160 nm. These emission wavelengths are typical for silicon nanocrystals of approximately $2-4$ nm in diameter.[19] The spectra are inhomogeneously broadened due to the size distribution of silicon nanocrystals in the floating gate. The steady state intensity of PL decreases for both positive and negative applied gate biases. This quenching effect is robust and reversible. We do not observe any change in the modulation amplitude after days of high intensity illumination and frequent voltage cycling. We attribute this suppression of PL to nonradiative Auger recombination in the presence of an excess charge either inside the nanocrystal or at a nearby interfacial trap state. Note that a slight blueshift (~ 10 meV) of the spectrum is observed for large negative gate biases. Because the spectrum is inhomogeneously broadened, a blueshift can be attributed to the preferential quenching of smaller band gap, larger diameter nanocrystals. This asymmetric quenching is only observed for the negative gate biases that we believe correspond to hole charging. We expect larger nanocrystals to be more readily charged than smaller nanocrystals because smaller bandgaps correspond to
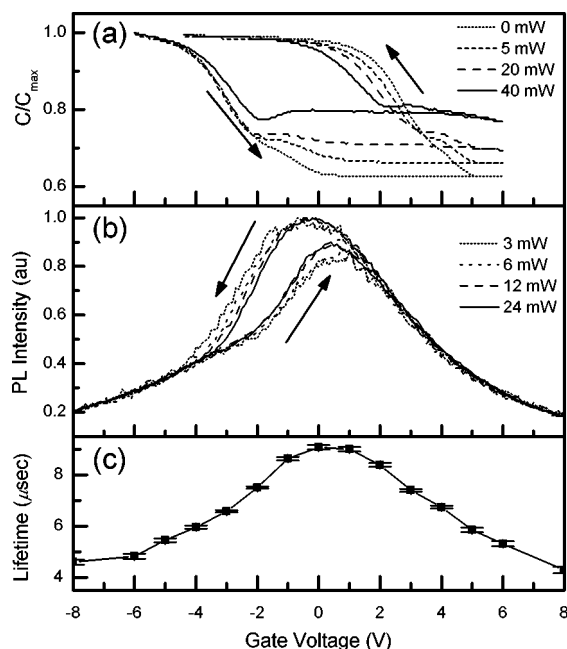
deeper energy wells to confine the stored charge. We can further speculate that internal photoemission obscures the observation of a blue shift for electron storage by reducing the proportion of electron-charged large nanocrystals in steady state.

In order to analyze the memory performance of the device, the gate bias was swept to record hysteresis curves. Figure 2(a) contains normalized capacitance–voltage $(C-V)$ electrical hysteresis traces for our memory device, in the dark and under laser illumination. The $C-V$ traces collected under illumination[20] show the inhibition of depletion due to optical carrier generation in the channel as well as the internal photoemission of stored electrons, which compresses the hysteresis away from positive gate biases. Assuming that charges are stored in the oxide according to a Gaussian distribution representative of the implanted silicon profile, we find that a sheet charge density of $\sim 2 \times 10^{12}$ q_e/cm^2 must be injected into the floating gate to change the threshold voltage by 1 V. We can therefore estimate a maximum sheet charge carrier density of $\sim 5 \times 10^{12}$ q_e/cm^2 in the oxide at the extremes of the hysteresis trace. This is close to the estimated lower bound on the nanocrystal density in the floating gate, suggesting that charge storage may saturate with an average of less than one charge carrier stored on each nanocrystal in the floating gate array.

In addition to the pronounced hysteresis in the $C-V$ trace, a significant optical hysteresis is observed in the PL intensity, as shown in Fig. 2(b). The presence of hysteresis in the optical trace is attributed to the quasinonvolatile storage of charge in the nanocrystals. As can be seen in Fig. 2(b), the width of the optical hysteresis is diminished under increasing illumination intensity, suggesting that the optical excitation reduces charge retention. The effect is particularly pronounced for positive gate biases that we believe correspond to electron storage on nanocrystals. We attribute the decrease
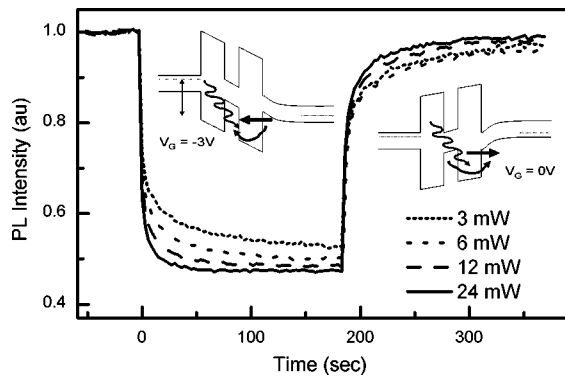
FIG. 3. PL response transient showing the evolution of the steady state response to a bias of −3 V at different excitation powers. Inset band structures are meant to schematically illustrate the dominant physical processes observed. The bias is switched off after 3 min and quenching persists for a characteristic retention time. The PL quenching shows a strong dependence on the optical excitation strength suggesting that optically assisted electrical programming occurs. Retention times of order 100 s are observed, which we attribute to the storage of holes within the nanocrystal array.

in retention time to internal photoemission processes that discharge carriers from the nanocrystals to the channel. The closure of the hysteresis loop is thus evidence for the optically assisted programming of nanocrystals. Closure seems to saturate with increasing pump intensity, indicating that a steady-state level of charge retention is approached. The optical hysteresis loop is superimposed on a trend of PL quenching that is symmetric in gate bias. This component of the PL quenching is attributed to nonradiative recombination paths related to volatile charge storage. These volatile quenching sites are assumed to be a consequence of nonidealities in our fabrication process.

PL decay traces in Fig. 2(c) were recorded at the emission peak of 760 nm at various gate biases and fit to stretched exponential functions, yielding experimental lifetimes from $4-9$ μs with the β parameter held constant at 0.7. These PL decay lifetimes are consistent with previous studies of nanocrystals fabricated by ion implantation.[21] The reduction in the PL decay lifetime under an applied gate bias is a signature of energy exchange between nanocrystals. We suggest that charged nanocrystals are rendered "dark" by Auger recombination and do not contribute to the recorded PL decay lifetime traces directly, but the remaining ensemble of neutral nanocrystals emit light with a reduced lifetime due to exchange of excitons with the "dark" charged nanocrystals. We can estimate that such an exchange occurs with a characteristic lifetime of about 10 μs at the extremes of applied gate bias, as the experimental PL decay lifetime is reduced by a factor of two.

To further investigate memory retention in our devices, we recorded PL transient response curves, in which the PL intensity is monitored at the peak of spectra recorded at 3 s intervals, while the bias condition is stepped from 0 V to a particular gate bias for several minutes and then returned to 0 V. Figure 3 shows such a transient response curve recorded for a −3 V gate bias at several illumination intensities. The data have been averaged over ten measurements and normalized to the initial steady state PL intensity. This gate bias is in the optically assisted programming regime,

where the illumination intensity has the greatest effect on the charging dynamics. Transient response curves recorded for gate biases of −6 V exhibit a sharp onset of PL quenching on time scales that will be addressed in further experiments.

We can see from the transient response curves that illumination at high intensity reduces the retention time of the memory device. This effect is attributed to optical erasure of the nanocrystals via internal photoemission, as indicated in the inset band diagram of Fig. 3. The efficiency of the photoemission erasure mechanism should increase with increasing excitation photon energy. Thus we would expect data retention to be maximized for the case of resonant excitation, which would be the least destructive read operation possible. Preliminary measurements in which the devices are pumped at wavelengths above 457.9 nm suggest that retention indeed improves.

In summary, we have demonstrated a silicon optical nanocrystal memory device fabricated via ion implantation that can be read and erased optical or electrically. Data retention times are of order 100 s. Measurement of the electrical programming speed was experimentally limited in this experiment to a resolution of 3 s.

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